711 E.S.L.

INSTRUCTION MANUAL

MODEL 750
PHASE METER

WAVETEK

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Serial No. _____

711

INSTRUCTION MANUAL

MODEL 750
PHASE METER

Product Improvement Notice

Wavetek maintains a continuing program to make improvements to their instruments that will take advantage of the latest electronic developments in circuitry and components.

Due to the time required to document and print instruction manuals, it is not always possible to incorporate these changes in the manual.

Wavetek has manufactured your instrument, using metal film 1% tolerance resistors in place of 5% carbon resistors, wherever practical. This results in a substantial improvement in the overall performance of your instrument. Therefore, there may exist a discrepancy between the resistor used to manufacture your instrument and the resistor called out in the Parts List and Schematic Diagrams in this manual.

If field replacement of an affected resistor does become necessary, replacement may be made in accordance with the manual call outs. Wavetek, however, recommends replacement with the same type of resistor used in the manufacture of your instrument, whenever possible.

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Figure i. Model 750 Phase Meter

SCOPE OF THIS MANUAL

This manual provides descriptive material and instructions for the installation, operation, maintenance, and repair of the WAVETEK Model 750 Phase Meter.

SECTION 1
INTRODUCTION

1.1 PURPOSE OF THE EQUIPMENT

The WAVETEK MODEL 750 PHASE METER has been designed to accurately measure the phase angle between any two ac signals (with an amplitude dynamic range as great as 2000 to 1) within the 10 Hz to 2 MHz range. A precision wideband bench instrument, the Model 750 uses a unique circuit design which permits accurate phase angle measurements with input signals having high even harmonic distortion. A four-digit readout is used to display, in degrees and tenths of degrees, the phase angle being measured.

Two ranges, 0°/360° and −180°/+180°, assure continuous phase data without discontinuity at 0 and 180 degrees. High impedance differential inputs are used; and a dc OUTPUT −10mV/DEG is provided for use in recording phase angle measurements, or as a control signal for phase lock loops or servo systems.

The automatic operation of this instrument eliminates the need for amplitude matching, frequency tuning, and output filtering, resulting in true hands-off operation.

1.2 GENERAL PHYSICAL DESCRIPTION

Weighing approximately 9 pounds (13 pounds when shipped) the Model 750 is 8½ inches wide, 5¼ inches high, and 10½ inches deep. Housed in a compact, ruggedized, portable case; the Model 750 is normally shipped with a 10-foot, 3-wire, detachable line cord and one copy of this instruction manual.

1.3 SPECIFICATIONS

1.3.1 Power Requirements

100-130 Vac or 200-260 Vac, 50-400 Hz, less than 25 W, single phase.

1.3.2 Input Signals

Frequency Range . . . . . 10 Hz to 2 MHz

OVERVOLTAGE LIMITS

Amplitude Ranges	AC Limit	Maximum Peak (AC + DC Limit)
.001-2 VOLTS RMS	50 V RMS	100 VOLTS
.300-300 VOLTS RMS	330 V RMS	500 VOLTS

Input Impedance
Single-Ended Inputs . . . . . 1 MΩ, shunted by 30 pF
Differential Inputs . . . . . 2 MΩ, shunted by 20 pF

Common Mode Rejection
10 Hz to 100 kHz . . . . . Greater than 50 dB
100 kHz to 2 MHz . . . . . Greater than 40 dB

1.3.3 Output Signals

OUTPUT −10mV/DEG (Standard)
Amplitude, 0°/360° Range . . . . . 0 Vdc to −3.600 Vdc
Amplitude, −180°/+180° Range . . +1.8 Vdc to −1.8 Vdc
Output Impedance . . . . . 1 kΩ

1.3.4 Accuracy

Absolute Calibration Accuracy
20 Hz to 20 kHz square wave, 100 mV to 5 V p-p . . . ±0.1°

Frequency Effect on Accuracy (100% of Range Sine Wave Inputs)
20 Hz to 20 kHz . . . . . Calibration Accuracy ±.2°
Zero Offset, 10 Hz to 10 kHz . . . . . Less than 0.1°
Zero Offset, 10 kHz to 100 kHz . . Less than 0.1°/10 kHz
Relative Accuracy, 100 kHz to 2 MHz . . . . Better than 2°

NOTE

The term relative accuracy means the accuracy of difference in phase reading from one condition to another. For example, it is the accuracy of 1) repeatability, 2) comparison of readings among unknown signals with respect to a given signal, 3) phase deviation of input without regard to zero offset.

Amplitude Effect on Accuracy (Equal Level Inputs)
Less than 1.5° for 60 dB change on both inputs
NOTE: Minimum sensitivity below 20 Hz and above 50 kHz is 1% of amplitude range.

Phase Angle Resolution . . . . . 0.1°

Phase Angle Drift . . . . . Less than .3° for 100 hrs.

Response Time (Full Scale Change) . . Less than 4 seconds

NOTES

1. *Phase angle measurements within 2° of the RANGE limits should be avoided; allow ±5° for frequencies below 50 Hz.*
2. *For frequencies above 20 kHz, both VOLTS RMS switches should be set to the same range to eliminate attenuator phase delay.*
3. *For operation at higher voltages, the instrument is designed for use with Tektronix or Hewlett Packard 10X probes.*

1.3.5 Mechanical Characteristics

Dimensions and Weight

Width . . . . . 8-1/2 inches
Height . . . . . 5-1/4 inches
Depth . . . . . 10-1/2 inches
Weight (Nominal) . . . . . 9 pounds
Weight (Shipping) . . . . . 13 pounds

Connector Types

Inputs . . . . . 3 Binding Posts, 3/4-inch spacing
Outputs . . . . . 2 Binding Posts, 3/4-inch spacing

1.3.6 Environmental Characteristics

Recommended Warmup 1/2-hour

Operating Temperature Range . . . . . 25°C (±5°C)

1.4 ACCESSORIES AND ASSOCIATED EQUIPMENT

The Model 750 is normally shipped with a 10-foot, 3-wire, detachable line cord and a copy of this instruction manual. The items listed below are compatible accessories and associated equipment which may be helpful in the user's installation.

Rack Adapter Kit . . . . . Wavetek No. 130-602
Attenuators, 10 to 1 . . . . . Dual Banana Jack Output
Single BNC Output
Adapters, Dual Banana . . . . . Dual Banana to BNC Plug
Dual Banana to BNC Receptacle
Shielded Test Leads, 36-inch . . Dual Banana to Dual Banana
Dual Banana to Alligator
Dual Banana to BNC

All phase angle measurements are dependent on type of waveform, amplitude, and frequency. The diagrams below show the absolute accuracy, taking into account all sources of error.

ABSOLUTE ACCURACY

ALL ACCURACIES STATED ARE ± DEGREES

CHANNEL A AMPLITUDE PERCENT OF FULL SCALE	.1%	1%	10%	100%
100%	2.4	1.5	0.7	0.4
10%	1.5	0.7	0.6	0.7
1%	0.7	1.0	0.7	1.5
.1%	1.5	0.7	1.5	2.4

CHANNEL B AMPLITUDE PERCENT OF FULL SCALE

The term relative accuracy means the accuracy of difference in phase reading from one condition to another. For example, it is the accuracy of 1) repeatability, 2) comparison of readings among unknown signals with respect to a given signal, 3) phase deviation of input without regard to zero offset.

MULTIPLICATION FACTOR
AS A FUNCTION OF FREQUENCY

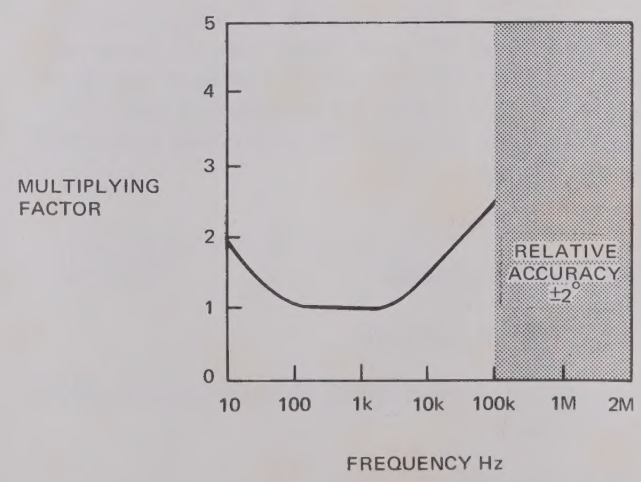


Figure 1-1. Instrument Accuracy Diagrams

SECTION 2
INSTALLATION AND OPERATION

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect the external parts for damage to knobs, indicators, connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

No mechanical installation is required when the instrument is to be used as a portable bench unit. If a rack mounting configuration, or a Rack Adapter Kit (see paragraph 1.4), is provided; the unit may be mounted in a standard 19-inch equipment rack. Instructions for attaching the Rack Adapter Kit are provided with the kit.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

Connect the ac line cord to the mating connector at the rear of the unit and the ac line supply. Check that the proper type of fuse is installed for the line supply being used.

NOTE

Unless otherwise specified at the time of purchase, the Model 750 is shipped from the factory with the power transformer connected for operation on a nominal 115-volt ac line supply. Conversion for 230-volt operation requires resetting a switch at the rear of the unit. To reset the 115/230 conversion switch (concealed by the rear panel) remove the rear panel, set the switch to 230 using a thin-bladed screwdriver, and replace the panel. Install a 1/8-ampere fuse in place of the normal 1/4-ampere fuse.

2.2.2 Input Connections

Connect the desired input signals to their respective connectors using shielded cable equipped with dual banana connectors. Connect single-ended inputs between ground and the appropriate polarity terminal, with the shorting link connected between ground and the opposite polarity terminal. Connect differential inputs between the "+" and "–" terminals, and disconnect the shorting link. See Table 2-1 for input connections and their requirements.

Table 2-1. ELECTRICAL INSTALLATION GUIDE

Symbol	Name	Function
J1	(Line Cord)	Connector for 3-wire line cord.
J2	INPUT A "+"	Connectors for single-ended or differential input signal. The shorting link is used only with single-ended inputs, between a polarized terminal and ground. Observe amplitude specifications and limits of paragraph 1.3.2. Use shielded cables with dual banana connectors for these connections.
J3	INPUT A "–"	
J4	INPUT A "⏚"	
J5	INPUT B "+"	Connectors for single-ended or differential input signal. The shorting link is used only with single-ended inputs, between a polarized terminal and ground.
J6	INPUT B "–"	
J7	INPUT B "⏚"	
J8	OUTPUT –10mV/DEG	Standard output connector.
J9	(Output "⏚")	

2.2.3 Output Connections

Connect the OUTPUT −10 mV/DEG to the desired point. Since the OUTPUT −10 mV/DEG has an output impedance of 1 kΩ the loading of this output should be considered. This output is short circuit proof and shorting it will not inhibit normal operation. See Table 2-1.

2.3 INSTALLATION CHECKS

This paragraph outlines a quick checkout procedure for determining proper operation of the instrument. Field calibration and checkout instructions are given in Section 4 for determining if the unit is within all electrical specifications. See Table 2-2 for a description of the functions of the operating controls. No special test equipment is required to perform a checkout of the instrument as outlined below.

1. Connect the line cord to the instrument and the line supply, depress POWER pushbutton, and allow a 20-minute warmup period for the unit to reach a stable operating temperature.
2. Depress RANGE 0°/360° pushbutton and hold CALIBRATE switch (on the rear panel) in the +360.0/+180.0 position. The four-digit readout should display "+360.0".
3. Hold CALIBRATE switch in the 000.0/−180.0 position. The four-digit readout should display "+000.0", ±000.1.
4. Depress RANGE −180/+180 pushbutton and hold CALIBRATE switch in the +360.0/+180.0 position. The four-digit readout should display "+180.0", ±000.1.
5. Hold CALIBRATE switch in the 000.0/−180.0 position. The readout should display "−180.0", ±000.1.

Table 2-2. OPERATING CONTROL FUNCTIONS

Symbol	Name	Function
SW1	POWER	Connects ac line voltage to the instrument.
SW2	115/230	Selector for 115-volt or 230-volt operation.
SW3	CALIBRATE	Used for quick check of offset (if any) in phase reading.
SW1	VOLTS RMS .001-2 (INPUT A)	When depressed, selects the 0.001 to 2 V rms input signal amplitude range for the A input. Interlocked with SW2 below.
SW2	VOLTS RMS .3-300 (INPUT A)	When depressed, selects the 0.3 to 300 V rms input signal amplitude range for the A input. Interlocked with SW1 above.
SW3	RANGE 0°/360° (A and B)	When depressed, the phase angle display range will be 0° to 360°, with slight discontinuity between 358° and 2°. Interlocked with SW4 below.
SW4	RANGE −180°/+180° (A and B)	When depressed, the phase angle display range is −180° to +180°, with slight discontinuity between 178° and 182°. Interlocked with SW3 above.
SW5	VOLTS RMS .001-2 (INPUT B)	When depressed, selects the 0.001 to 2 V rms input signal amplitude range for the B input. Interlocked with SW6 below.
SW6	VOLTS RMS .3-300 (INPUT B)	When depressed, selects the 0.3 to 300 V rms input signal amplitude range for the B input. Interlocked with SW5 above.

If, after sufficient warmup, the proper readings are not observed, refer to the Calibration Instructions given in paragraph 4.2 of this manual.

2.4 OPERATING CONTROLS

The operating controls and the functions they perform are given in Table 2-2. Additional adjustments, and the functions they perform, are described as they appear in the text of Section 3 and Section 4 of this manual. Do not disturb any control settings, with the exception of operating controls, unless absolutely necessary; and then only if suitable equipment is available for recalibration.

If the equipment appears to operate abnormally, refer to the Calibration Instructions (paragraph 4.2) and the Corrective Maintenance (paragraph 4.3) instructions.

2.5 OPERATING PROCEDURE

No preparation for operation is required beyond completion of the initial Installation Checks given in paragraph 2.3 of this manual.

CAUTION

If single-ended ac inputs are used, the shorting link must be connected between the negative and ground terminals. If differential ac inputs are used, the shorting link must be removed and the input signal must be connected between the positive and negative (+ and −) terminals.

CAUTION

To measure the phase angle between any two ac signals (with an amplitude ratio as great as 300,000 to 1) within the specified frequency range, proceed as follows:

1. Depress the appropriate VOLTS RMS pushbutton for each input signal.
2. Depress the appropriate RANGE pushbutton to select the range (0/360 or −180/+180) that provides the closest center of range indication, or use both ranges for continuous phase angle measurements.
3. Connect one ac signal to INPUT A terminals and the other signal to INPUT B terminals observing the CAUTION notice above.

NOTICE

If the readout jumps or scatters occasionally with low input amplitude and/or frequency, it is probably caused by noise spikes riding on the input signal or a high signal to noise ratio. To eliminate or reduce this effect connect a 0.1 μF capacitor (or matched filters) across input terminals.

NOTICE

4. Read phase angle (phase difference) directly on digital display panel. If the readout polarity is positive, INPUT B leads INPUT A by the measured number of degrees. If the readout polarity is negative, INPUT B lags INPUT A by the measured amount.
5. OUTPUT −10mV/DEG provides the same data, electronically, for use as a control signal or for general recording applications.

SECTION 3
CIRCUIT DESCRIPTION

3.1 SIMPLIFIED BLOCK DIAGRAM

As shown in Figure 3-1, the Model 750 Phase Meter consists of two similar input channels (only the A channel has the RANGE selector switch) and a common output channel. Paragraph 3.2 provides further descriptions of the functions of each basic circuit comprising this instrument. This paragraph describes, briefly, the major circuit elements and their relationship to one another.

The Frequency Compensated Attenuator in each input channel is used to reduce high amplitude inputs to a level

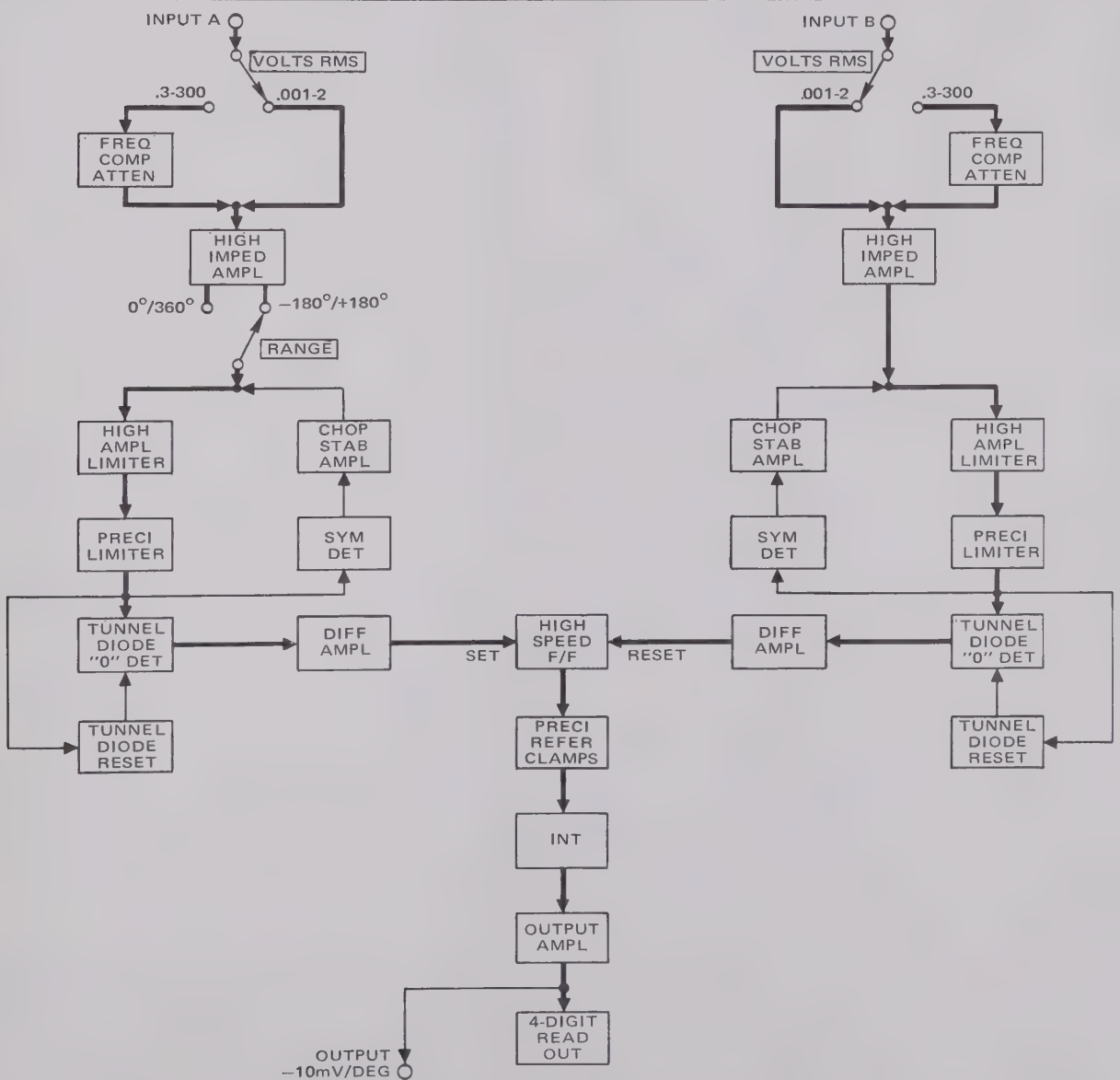


Figure 3-1. Simplified Block Diagram

suitable for the remaining circuitry. The attenuator is in the circuit when the .3-300 VOLTS RMS input range is selected, and it is out of the circuit when the .001-2 VOLTS RMS range is selected.

The selected input signal is applied, through the VOLTS RMS switch, to a High Impedance Amplifier stage. In the A channel, the RANGE switches (0°/360° or −180°/+180°) select the appropriate phase out of the differential amplifier. The B channel does not employ a 180° phase shifter, as only one is needed in the instrument. Another function of the High Impedance Amplifier is to isolate the plus and minus inputs and provide high common mode rejection.

Next, the signal is high-amplitude-limited to prevent overdriving in the Precision Limiter stage. The Precision Limiter is a nonlinear feedback, wideband amplifier which limits the input signal at ±100 μV. The limited output signal is applied to a Symmetry Detector which integrates the waveform and produces a dc voltage that is proportional to the symmetry of the clipped waveform. This dc output represents an error in the zero-crossing system or an error due to the distortion of the input signal. The dc level is amplified and inverted in a Chopper Stabilized Amplifier and summed at the input to the first limiter stage. The closed-loop circuitry provides long-term, stable phase detection and automatically balances the limiters to correct for drift or offset voltages in the system due to temperature variations or component aging. Errors due to even-harmonic distortion are essentially eliminated by this self-balancing zero-crossing technique.

Following the limiters, the waveform zero-crossing is detected in a wideband Tunnel Diode Zero Detector. The Tunnel Diode Reset supplies the reset signal to the detector and provides system noise immunity. The detected zero-crossing output is then applied to the High Speed Flip-Flop through a Differentiating Amplifier. The output of Channel A is applied to the "set" input, and the output of Channel B is applied to the "reset" input of the flip-flop.

The flip-flop output is applied to a Precision Reference Clamp stage which provides a signal having an amplitude defined by the reference voltage and a duty cycle proportional to the phase difference between the two input signals. This output is integrated into a dc voltage proportional to the phase difference and is applied to the Output Amplifier for full scale and zero adjustment, before being applied to the digital display readout and output connectors.

3.2 FUNCTIONAL BLOCK DIAGRAM ANALYSIS

As each functional circuit is described, refer to the appropriate block diagram and, if necessary, the appropriate portions of the schematic diagrams at the rear of this manual.

3.2.1 Zero Crossing Circuit (Figure 3-2 and 3-3)

Both input channels employ similar Zero Crossing Circuits; the only difference being the RANGE switch in Channel A. In view of this, only the functions of Channel A are described, realizing that there are counterparts in Channel B. Figure 3-2 is a functional block diagram of the Zero Crossing Circuit, Figure 3-3 shows key waveforms within this circuit.

When .001-2 VOLTS RMS is selected as the input amplitude range, the input signal is capacitively coupled to the High Impedance Differential Amplifier Q1-Q2. When the .3-300 VOLTS RMS range is chosen, the input signal is passed through the Frequency Compensated Attenuator before being applied to Q1-Q2. When the latter range has been selected, the plus and minus inputs are symmetrically attenuated in the ac/dc attenuator which is adjusted for a flat frequency response by trimmer capacitors C1 and C5.

The input source currents for the High Impedance Differential Amplifier stage are balanced by trimmer adjust R187 to yield best common mode rejection. The output of Q1-Q2 is applied, through the selected RANGE switch, to either the positive or the negative input of Input Amplifier IC1.

Trimmer capacitors C10 and C11 adjust the phase shift of the negative and positive inputs to IC1 to match those of IC4 in Channel B for best high frequency performance. IC1 provides either a 180° or a 0° phase shift, depending on the setting of the RANGE selector switches. With either range the gain of IC1 is unity, and its output is applied to the summing junction at the gate of Q3. FET Q3 and transistor Q4 provide a high input impedance to the summing point, as well as temperature compensation. The output from Q3-Q4 is applied to the symmetrical Amplitude Limiter CR1-CR4. R21 is used to balance this four-diode limiter.

The output from CR1-CR4 is coupled to Precision Limiting Amplifier IC2, a 50 MHz amplifier with nonlinear feedback. R28 is a dc balance adjustment, C22 is a phase matching trimmer. The output of IC2 is a clipped waveform having an amplified volts/second relationship at the zero crossing of the input waveform.

For high accuracy, the output of the final limiting amplifier of a zero crossing system must be symmetrical for a sine wave input. To ensure this, the output waveshape must be sampled periodically and the result fed back to the input of the first limiter to correct any unbalance or dissymmetry. The Integrator (comprised of R37-R40 and C26 and C30)

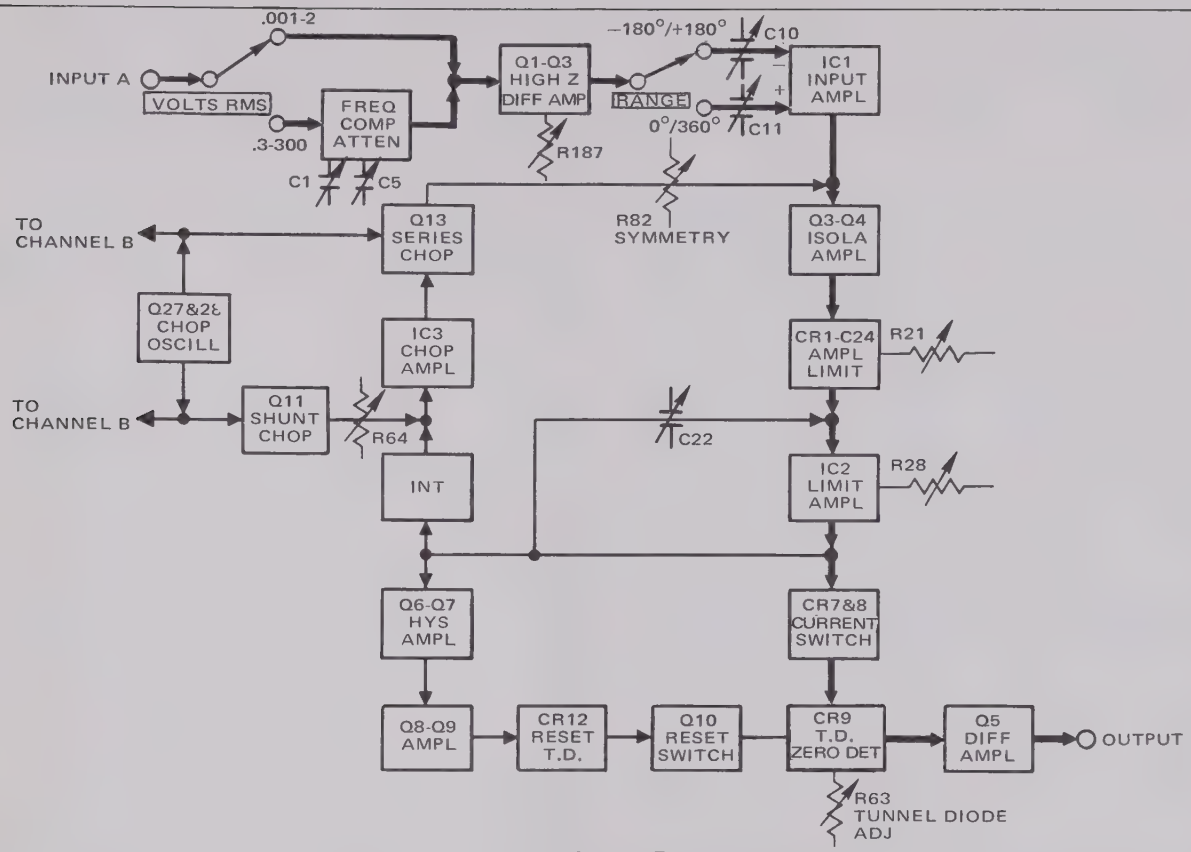
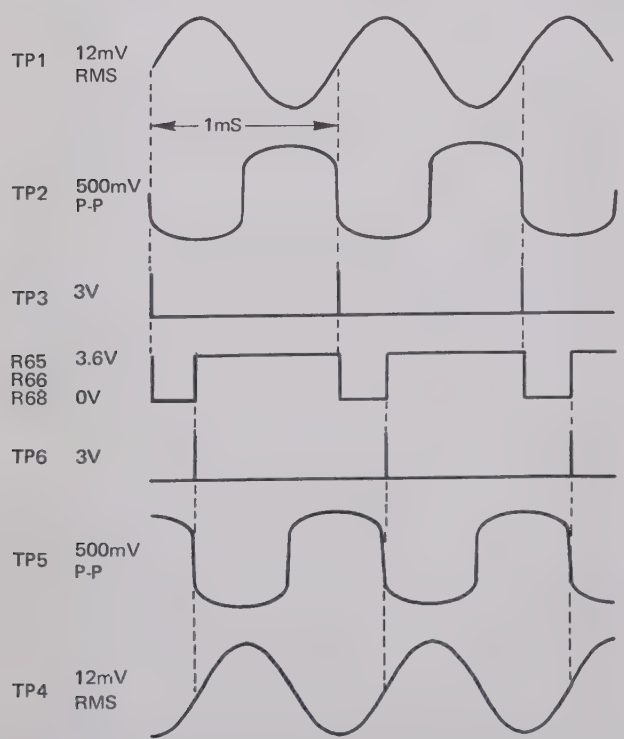


Figure 3-2. Zero Crossing Circuit, Functional Block Diagram



NOTES

A and B VOLTS RMS	.001-2V
PHASE RANGE	0°/360°
INPUTS	10mV RMS

CHANNEL B LAGS BY 90°

Figure 3-3.
Timing Diagram, Zero Crossing, and Logic Circuit

supplies a dc voltage proportional to the symmetry of the output of IC2 to the input of Chopper Amplifier IC3. Shunt Chopper Q11 converts the dc output of the Integrator to an ac signal. R64 is the chopper balance adjust.

This ac signal is then amplified in IC3, and the output is demodulated in Series Chopper Q13. The voltage developed across capacitor C59 is an amplified error signal proportional to the nonsymmetry of the output of IC2. This error signal is applied, through R23, to the summing point at the gate of Q3. R82 is a symmetry adjustment which controls the amount of error signal in the feedback loop. This chopper-stabilized symmetry-detection system also eliminates the effects of even harmonic distortion with the limits of the chopper loop.

The symmetrical output of IC2 is then applied to Current Switch CR7-CR8 which supplies a small amount of current, at the actual zero crossing point, to trigger Tunnel Diode Zero Detector CR9. Tunnel Diode Adjust R63 sets the firing point of CR9 to be at the zero crossing point.

Differentiating Amplifier Q5 then supplies a pulse output which occurs at the true zero crossing point of the input waveform.

The reset circuitry for CR9 consists of transistors Q6 through Q10. Hysteresis Amplifier Q6-Q7 amplifies the output of IC2 and provides the necessary hysteresis to prevent double triggering. The output from Q6-Q7 is applied, through Amplifier Q8-Q9, to reset Tunnel Diode CR12. When CR12 fires, the resultant waveform is differentiated and drives Reset Switch Q10 to saturation which, in turn, resets the Tunnel Diode Zero Detector CR9 to its original state.

Chopper Oscillator Q27-Q28 is the circuitry common to both channels of the Zero Crossing Circuit. This oscillator supplies the chopper pulse which drives the gates of field-effect-transistors Q11 and Q13 at the proper sample rate.

3.2.2 Logic Circuit (Figure 3-3 and 3-4)

The Logic Circuit converts the pulse information generated by the Zero Crossing Circuit into a precision, linear dc voltage whose value is a direct function of the phase difference between inputs A and B.

The two pulses generated by the Zero Crossing Circuit are applied to the inputs of a fast rise and fall time Set-Reset Toggle IC4. This stage is a dual transistor gate connected as an RS toggle with hot carrier diodes CR13 and CR14 providing nonsaturated, high speed operation. This stage

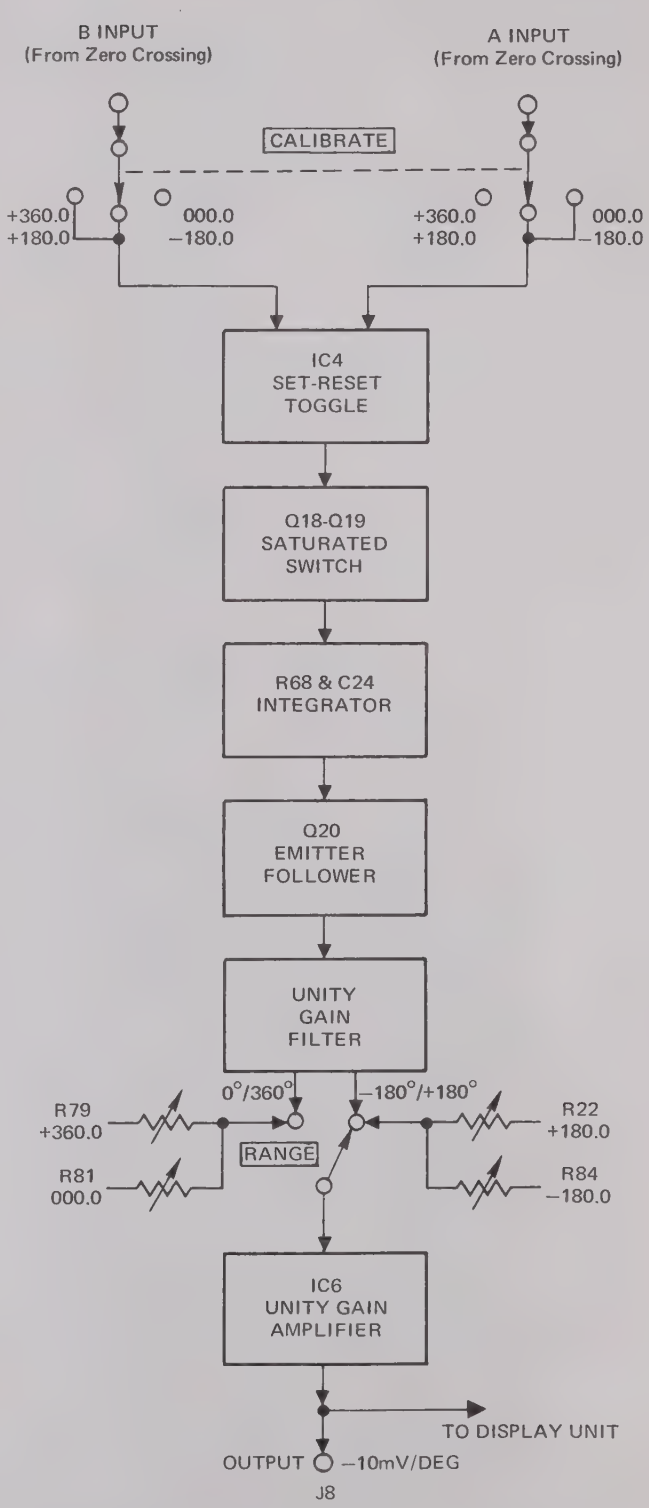


Figure 3-4. Logic Circuit, Functional Block Diagram

converts the pulse information into a rectangular waveform that drives Saturated Switch Q18-Q19.

When the CALIBRATE switch is actuated, it inhibits either the "A" or "B" input from the Zero Crossing Circuit. With one input inhibited, the Set-Reset Toggle IC4 will go to a single state and remain. One state of IC4 corresponds to 0°, the other state corresponds to 360°. Therefore, when CALIBRATE switch SW3 is actuated, all dc calibrations may be checked.

Q18-Q19 operates as a pair of saturated switches between ground and a precision +3.6 Vdc. The resulting output, at the junction of R65 and R66, is integrated in Integrator R68/C24 and then filtered by an active Unity Gain Filter comprised of IC5, R69, R70, C25, and C26. Q20 functions as an Emitter Follower input to the Unity Gain Filter.

The integrated and filtered signal, representing the phase angle between INPUT A and INPUT B, is then conditioned in the Unity Gain Amplifier IC6. The final dc voltage out of IC6 has a −10 mV/degree relationship to the measured phase angle, and is provided (at J8) as an output as well as the input to the Digital Display Circuit.

RANGE calibration is accomplished by four potentiometers at the rear of the unit. When the 0°/360° RANGE is selected, the +360.0 and 000.0 limits may be calibrated using R79 and R81 respectively. When the −180°/+180° RANGE is selected, the +180.0 and the −180.0 limits may be calibrated using R22 and R84 respectively.

The reference voltage at the integrator input is the same voltage used as the voltmeter reference. The result is a ratio measurement that is independent of power supply drift.

3.2.3 Digital Display Circuits (Figure 3-5 and 3-6)

The Digital Display Circuit is a four-digit, automatic-polarity-indicating, dual-slope-integrating, digital voltmeter (DVM). As this circuit is described, refer to the timing diagram (Figure 3-6) as well as the block diagram and schematic at the rear of this manual.

The −10 mV/degree dc output from the Logic Circuit is applied to the input of the Digital Display Circuit. This input is switched into an integrator for a precise time interval, causing the integrator to "ramp" to some voltage. At the end of the input time interval, a reference voltage is switched into the integrator causing it to ramp back to zero. The time between the start of the reference ramp and the time the reference ramp passes through zero is converted to a timing pulse by logic circuitry. The width of this pulse is directly related to the amplitude of the dc voltage input applied to the DVM, and thus, the phase relationship (phase angle) of INPUT A to INPUT B. This pulse is used to gate a counter so that, for each 1 mV of input voltage, one count is displayed, yielding .1° phase resolution on the digital readout.

The entire DVM is synchronized from a master clock, Oscillator IC7-Q17, which is scaled down in the four 10^N Decade Counters, to provide the DVM time base. This time base controls the input to the Integrator, IC1, and sequences logic decisions used to generate the counter gating pulse.

The Integrator, IC1 and C2, has four inputs. The input voltage is switched in by Q1 and Q2. Depending on the input voltage polarity, either the +3.6 V reference is switched in by Q3 and Q4, or the −3.6 V reference is switched in by Q5 and Q6. Zero adjustment is made by R11 (ZERO OFFSET ADJ) which compensates for the input switch and integrator offset voltages.

It should be noted here that the +3.6 V used as the DVM reference is also the +3.6 V used to power the circuitry generating the dc output from the Logic Circuit. Thus, if the +3.6 V should change, there will be virtually no variation in the DVM output since a ratio relationship exists between the generating source and the measuring system.

The output of IC1 is detected in Comparator IC2 and the Amplifier comprised of Q8-Q10. IC3A and IC4A provide additional drive for the comparator input at zero, through Q7 and Q11, to prevent multiple comparator outputs. The amplified comparator output steers JK Flip-Flop IC5A which, upon receipt of the 10^{-3} 8 clock signal from IC5B, determines the polarity of the DVM input voltage. Once the polarity has been determined, either IC3B or IC4C changes state to switch in the appropriate reference voltage for ramping the integrator back to zero. As the reference voltage is switched in, IC3C is gated positive, producing the start of the output pulse. When the Integrator reaches zero, the Comparator changes state. This change in state causes IC3B or IC4C to gate IC3C negative, generating the end of the output pulse.

The analog board converts the dc output of the phase meter to a positive pulse whose width is proportional to the phase shift at the input to the instrument. This pulse is then applied to pin 4 of the Digital Readout Board.

The positive pulse is fed through R3 to the base of Q2, an inverter, causing the collector of Q2 to go negative for the same duration. The first negative transition of the pulse at the collector of Q2, coupled through C1, causes the output of IC2 to go positive. This positive output is applied to the reset pins of IC5, IC8, IC11, and IC14—the counter portion of the digital readout

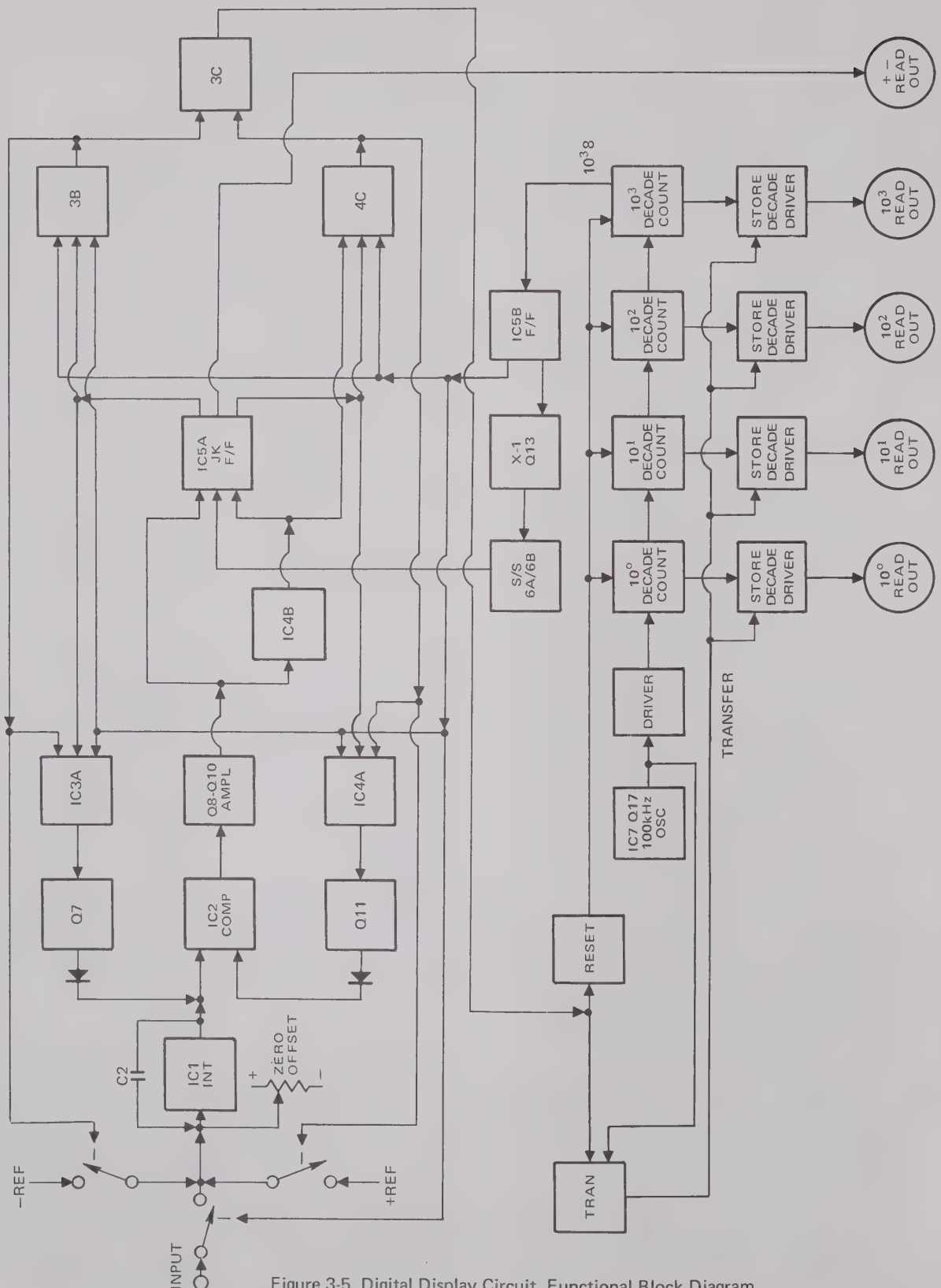


Figure 3-5. Digital Display Circuit, Functional Block Diagram

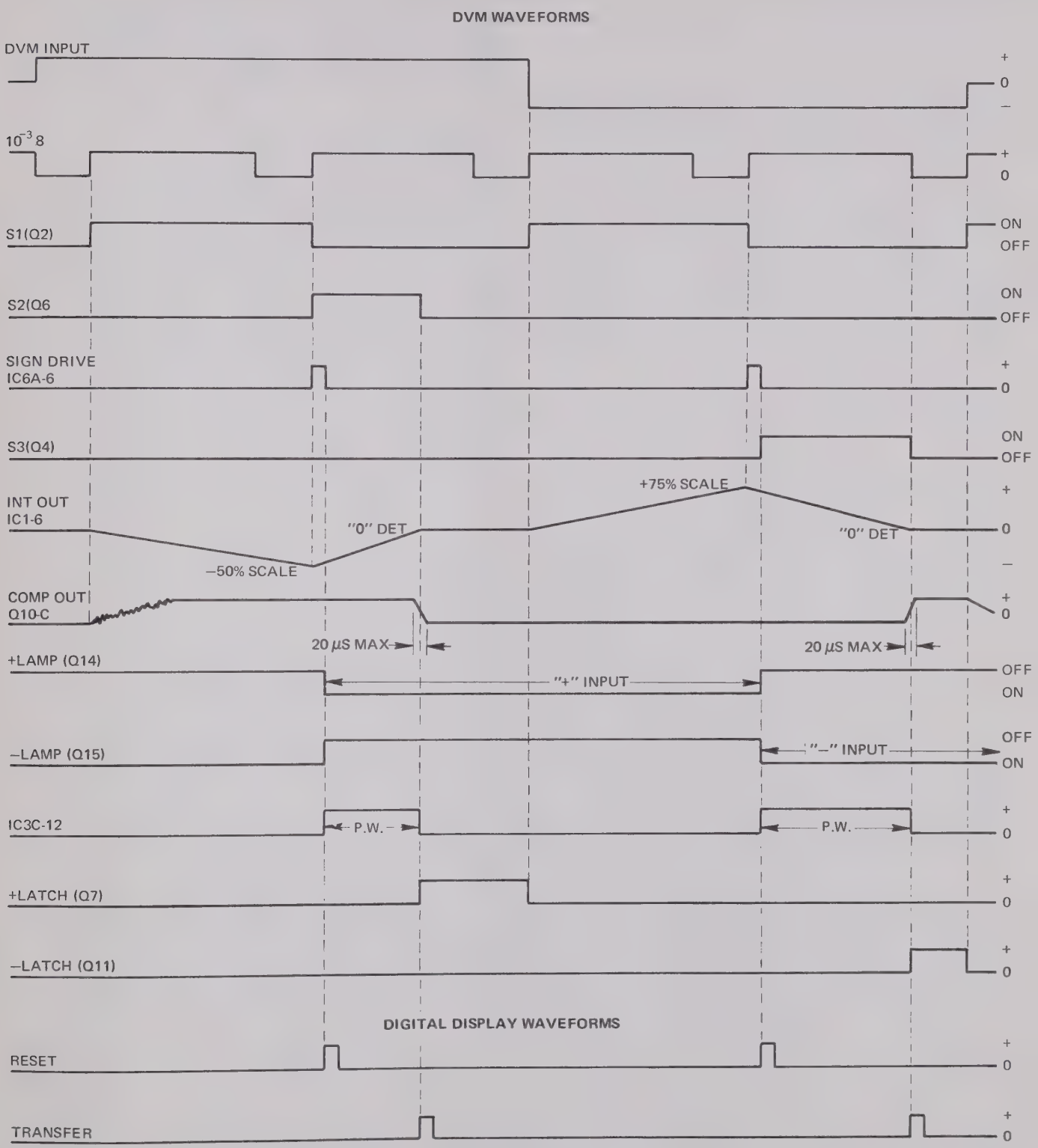


Figure 3-6. Digital Display Circuit, Timing Diagram

system. Thus, the negative transition of the pulse at the collector of Q2 causes a zero state to be set into the counter.

The clock input, a frequency of approximately 25 kHz, is applied through Q1 to pin 14 of IC5, the first decade of the decade counter stages. This frequency is then counted until a positive transition of Q2 is coupled through C2 causing IC2 to go negative. The single-shot configuration of IC2 provides a positive pulse at pin 8. This also drives pin 1 of IC1 to a positive condition which (if pins 8 and 11 of IC1 are in the reset condition) allows the pulse to get through to pin 3 of IC1 and pin 6 of IC1 to go negative. This action strobes the information from the clock decade counters into the latch circuits of IC4, IC7, IC10, and IC13, and also strobes the Print Command output circuit.

When the new information is updated into the quad latch circuitry, decoder drivers IC3, IC6, and IC9, and IC12 then decode the information and present it to the digital display tubes V1, V2, V3, and V4.

Transistors Q3 and Q4 are the plus and minus sign drivers for the digital display tubes.

Due to the cycle time of the dual slope integrator; the maximum waiting period, from input of an external read command to output of a print command and the data presented to the digital readout is approximately 1 second.

3.2.4 DC Power Supplies (Figure 3-7)

Regulated operating voltages for the Model 750 Phase Meter include +15 V, −15 V, +3.6 V, −3.6 V, +5 V, and

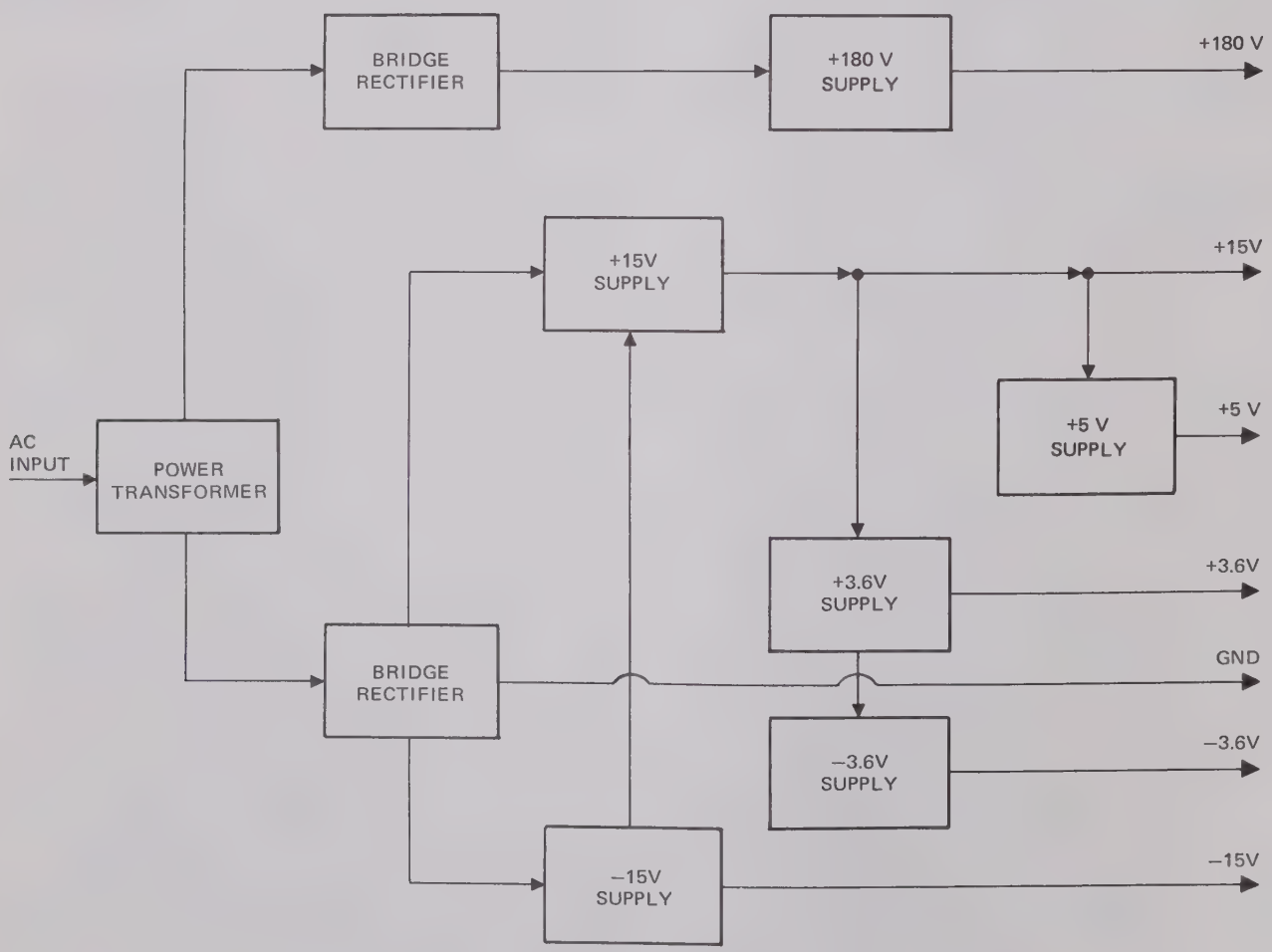


Figure 3-7. DC Power Supplies, Functional Block Diagram

+180 V. AC line voltage is connected through the line cord to the POWER switch on the front panel. A slo-blo fuse is installed on the line side of the switch, and a 115/230 power selector switch connects the primary winding of the power transformer for the appropriate line voltage.

AC voltage is coupled from the transformer secondary to the Bridge Rectifier CR1-CR4. Filtering is provided by C3 and C11. Q12 is operated as a Zener diode reference voltage for the −15 V supply. IC3 is a comparator differential amplifier. The Comparator drives a Darlington-connected Series Pass transistor pair, Q9 and Q11, used for added current gain. Q8 is also connected to operate as a Zener diode reference to provide a voltage level shift for the output of IC3. R36, −15 V ADJ, adjusts the minus input of IC3 with respect to the plus input which has a Zener voltage of approximately 7 volts. If the −15 V tries to increase due to a change in line voltage or load current, the collector of Q12 stays approximately at the same voltage. Thus, the minus input to IC3 becomes more positive than the plus input, and the IC3 output draws more current. The output moves less positive, and this change is coupled to the base of Q9 and Q11 through Q8, returning the supply to −15 volts.

IC1 is a Comparator Differential Amplifier in the +15 V supply. The plus input of IC1 is returned to ground through R9. Voltage Divider R7-R8, between the plus and minus 15-volt supplies, sets the minus input of IC1 precisely at ground. An increase in the −15 volts, due to line voltage variation or load current change, results in the minus input of IC1 moving positive, and the output of IC1 moving negative. This change is coupled to the bases of Q1 and Q2 through Q4. Q1 and Q2 form a Darlington-connected Series Pass pair for added current gain. The negative-going change returns the output to +15 volts.

Q3, in conjunction with R2 through R4, comprises a foldback current limiter for the +15 V regulator. Normally, the base of Q3 is turned off. Thus, the base of Q2 moves freely as the output from IC1 changes. When the +15 volt output is overloaded, heavy current flows through R2 and creates a potential drop across the resistor. When the potential drop overcomes the drop across R3, Q3 begins to conduct, starting to short the base of Q2 to the +15 volt output. In this condition, the output can be shorted indefinitely at a lower than maximum power dissipation of Q1. When the overload condition is removed from the +15 V output, the base of Q2 starts to rise. As the emitter of Q1 rises toward +15 volts, Voltage Divider R3-R4 has more effect on the base of Q3 and eventually turns Q3 off completely. When Q3 turns off, the normal condition is restored. Q10 with R28, R29, and R30, form a foldback current limiter for the −15 volt regulator.

The +3.6 volt supply is provided by Q5 and Q6 operating as a Comparator Differential Amplifier controlling the Series Pass transistor Q7. The error signal is obtained from the wiper of R20, in a Voltage Divider comprised of R18, R20, and R21 between +3.6 volts and −15 volts (the −15 volts here acts as a reference voltage) and R2 is used as the +3.6 volt adjustment.

The −3.6 volt supply is provided by IC2 operating as a Unity Gain Operational Amplifier with R22 providing gain control and the −3.6 volt adjustment.

For the +5 volt supply, ac voltage is coupled from the transformer secondary to Bridge Rectifier CR8-CR11. Filtering is provided by C14. Q14, Q15, and Q16 form a Comparator Differential Amplifier controlling Series Pass transistor Q13. The error signal is sensed directly on the +5 volts and is applied to the base of Q16. The Voltage Divider R38-R44, between +15 volts and ground, provides the reference voltage for the base of Q15. Q17, R40, R41, R42, and R43 form a foldback current limiter for the +3.7 volt regulator.

For the +180 volt supply, ac voltage is coupled from the transformer secondary to Rectifier CR12. Current limiting is provided by R48 and filtering is provided by C17. R49 is a bleeder resistor for C17, to prevent a sustained high voltage after power is turned off.

3.3 SUPPLEMENTAL CIRCUITS

There are no unique or supplemental circuits within the Model 750 to be separately described as "Supplemental Circuits". The preceding circuit descriptions adequately describe the complete circuitry of the Model 750 to the degree required by a competent technician.

SECTION 4
MAINTENANCE

4.1 ACCESS INSTRUCTIONS

Removal of the dust cover affords quick access to the majority of components within the unit. However, it may be necessary to remove the Digital Readout Assembly or the Zero Crossing Board in order to gain access to those components not exposed by removing the dust cover. Instructions for all three are given below.

4.1.1 Removing the Dust Cover

To remove the dust cover (case) from the Model 750 Phase Meter, the following procedure should be followed.

1. Unplug the power cord.
2. Unscrew two captive screws on rear panel.
3. Remove rear casting.
4. Set instrument face down and, watching clearance between bottom printed circuit board and cover, lift cover off slowly making sure bolts on the cover do not hit any adjustments.
5. Reverse this procedure when replacing dust cover. Tighten the captive screws only finger-tight.

4.1.2 Removing the Digital Readout Assembly

To remove the Digital Readout Assembly from the Model 750 Phase Meter, proceed as follows:

1. Remove the two Phillips screws on top of the Digital Readout Assembly closest to the front panel.
2. Remove the two Phillips screws holding the two bars extending from the assembly to the rear panel.
3. The assembly can now be removed and placed on the POWER switch side of the instrument. The unit may be turned on and operated while in this stage of disassembly.
4. The assembly may be completely removed by lifting up on the AMP pins connecting the assembly to the Logic and Power Supply board.

4.1.3 Removing the Zero Crossing Board

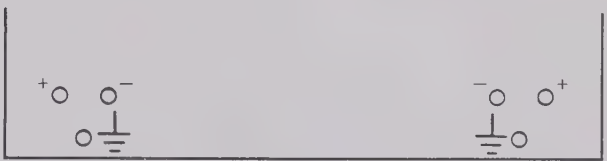
To remove the Zero Crossing Board from the Model 750 Phase Meter, proceed as follows:

1. Set instrument on its side and disconnect the AMP pins of the two sets of three input connectors. These are located near the front of the bottom board.
2. Remove the three bottom screws on both sides of the instrument holding the Zero Crossing Board to the side plates.
3. Slide Zero Crossing Board back until front switches clear the front panel.
4. Swing the Zero Crossing Board out from the front and replace the screws at the rear of the board. This allows the user to get at both sides of the Zero Crossing Board while the instrument is operating.

NOTE

The inputs are now available at the AMP pins on the front of the Zero Crossing Board.

5. To replace the Zero Crossing Board, reverse the above procedure. When reconnecting the input AMP pins, follow the diagram below.



Component Side of Zero Crossing Board

4.2 CALIBRATION INSTRUCTIONS

This paragraph provides complete sequential calibration instructions for the Model 750 Phase Meter. The instructions are concise and are written for the experienced electronics technician or field engineer having a working knowledge of this type of instrumentation.

WAVETEK maintains a factory repair department for those customers not possessing the necessary test equipment or personnel to maintain this type of instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached. This will hasten turnaround time.

Test point and control locations necessary for calibration are given within this section unless a foldout illustration is required. In the latter instance, the foldout illustration will be found at the rear of the manual.

4.2.1 Recommended Test Equipment

The following test equipment (or equivalent) is recommended for this calibration procedure.

VCG/VCA Generator	Wavetek Model 136
Voltmeter	1mV Resolution
Oscilloscope	Tektronix Model 454
Flat-bladed screwdriver	1/8-inch

4.2.2 Preliminary Procedures

Before attempting to recalibrate this instrument, the user should read and understand the entire calibration procedure. The four major segments of this procedure should be performed in the sequence given, as should the steps within each segment.

1. Connect the Model 750 Phase Meter in the test set up illustrated in Figure 4-1[A].
2. Set POWER switch to ON, set RANGE selector for 0°/360°, and set both VOLTS RMS selectors for .001-2.

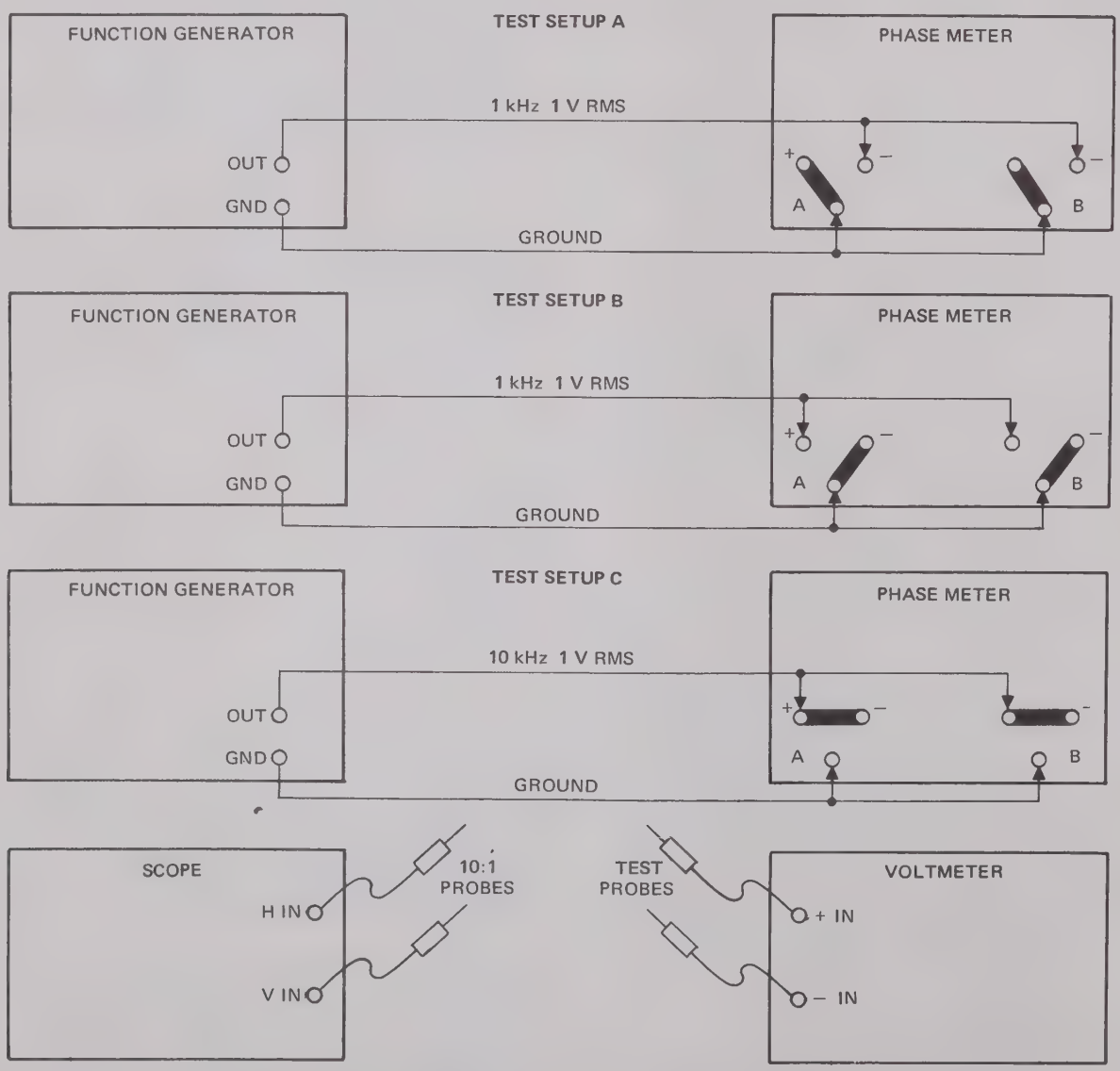


Figure 4-1. Calibration Set-Up

3. Allow a 30-minute warmup period before attempting to calibrate this instrument.

4.2.3 Full Scale Calibration Procedure

4. With equipment connected as shown in Figure 4-1[A]; hold CALIBRATE switch down (000.0/−180.0) and adjust 000.0 ADJ R81 for 000.0 plus or minus 1/2-count.

NOTE

One-half count (1/20th of a degree) can be determined by interpolation of alternate readings. If display alternates between ±000.0 and +000.1, the indication may be averaged to give +000.05. Careful adjustment should yield a display of ±000.0 (±.1) after equipment warmup.

5. Hold CALIBRATE switch up (+360.0/+180.0) and adjust +360.0 ADJ R79 for a display centered between +359.9 and +360.0.
6. Set RANGE selector for −180°/+180°.
7. Hold CALIBRATE switch down (000.0/−180.0) and adjust −180.0 ADJ R84 for a display centered between −179.9 and −180.0.
8. Hold CALIBRATE switch up (+360.0/+180.0) and adjust +180.0 ADJ R22 for a display centered between +179.9 and +180.0.
9. Repeat steps 4 through 8 for best indications. If all four calibrations are not within the specified limits, refer to the Logic Board Calibration Procedure given in paragraph 4.2.4.

4.2.4 Logic Board Calibration Procedure

10. Remove the dust cover and the display unit from the Model 750 Phase Meter following the procedures outlined in paragraphs 4.1.1 and 4.1.2.
11. Connect the positive probe of the voltmeter to test point TP2, and the negative probe to TP1, of the Logic Board (Figure 4-2).
12. Set POWER switch to ON and allow a 30-minute warmup period.
13. Set RANGE selector to 0°/360°, and set +3.6 V ADJ R20 to the center of its adjustable range.
14. Adjust −15 V ADJ R36 to obtain +3.600 V (±2 mV) between TP1 and TP2 (+3.6 V supply).
15. Connect the voltmeter to the OUTPUT −10mV/DEG and GROUND dual-banana terminals (J8 and J9) at the rear of the instrument.

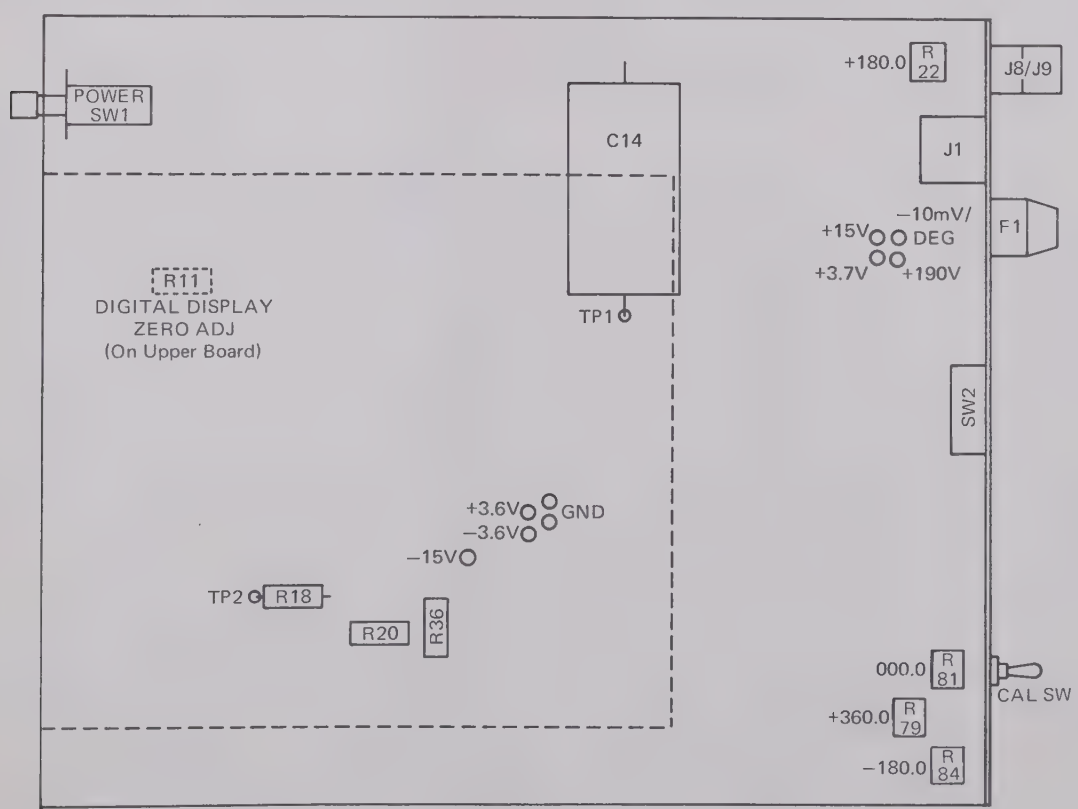


Figure 4-2. Logic Board Adjustment Locations

16. Hold CALIBRATE switch down (000.0/−180.0) and adjust 000.0 ADJ R81 for 0.000 V (±.3 mV) on the voltmeter.
17. Hold CALIBRATE switch down (000.0/−180.0) and adjust DIGITAL DISPLAY ZERO control R11 (accessible from the left side of the top printed circuit board of the Digital Display assembly) for a display of 000.0 plus or minus 1/2-count.
18. Hold CALIBRATE switch up (+360.0/+180.0) and adjust +360.0 ADJ R79 for a display centered between +359.9 and +360.0.
19. Hold CALIBRATE switch up (+360.0/+180.0) and adjust +3.6 V ADJ R20 for −3.600 V (±.3 mV) on the voltmeter.
20. Set RANGE selector to −180°/+180°.
21. Hold CALIBRATE switch down (000.0/−180.0) and adjust −180.0 ADJ R84 for a display of −180.0 plus or minus 1/2-count. Voltmeter should read +1.800 V ±2 mV.
22. Hold CALIBRATE switch up (+360.0/+180.0) and adjust +180.0 ADJ R22 for a display of +180.0 plus or minus 1/2-count. Voltmeter should read −1.800 V ±2 mV.
23. If readings are within ±2 mV, turn power off and reinstall display.
24. If steps 16 through 22 are out more than ±2 mV on the voltmeter, repeat steps 14 through 22 again. If voltmeter still indicates readings outside the specified limits, refer to the Corrective Maintenance instructions in paragraph 4.3.

4.2.5 Zero-Crossing Mid-Frequency Procedure

25. Turn power on, set both VOLTS RMS selectors to .001-2, and set RANGE selector to −180°/+180°.
26. Connect a 1 kHz sine wave, 10 mV rms (28 mV p-p), into each input (Figure 4-1[A]).
27. Check 10:1 oscilloscope probe for dc zero, by connecting it to the GROUND banana jack, and center trace on horizontal centerline of CRT. Set scope gain to 10 mV/centimeter, and sweep speed to 0.1 ms/centimeter.
28. Connect the scope probe to Channel A test point TP2 (Figure 4-3) of the Zero Crossing Board. The oscilloscope should display a waveform similar to the one shown in Figure 4-4[A].
29. Adjust DC BALANCE ADJ R28 so that V1 (Figure 4-4[A]) is equal to V2 (±10 mV).
30. Adjust CHOPPER BALANCE ADJ R64 so that t_1 (Figure 4-4[A] is equal to t_2 (±1 μS).
31. Alternately perform steps 29 and 30 until the closest to optimum results are obtained.
32. Adjust TD ADJ R63 until top of tunnel diode trigger is at zero volts dc (±1 mV) as shown in Figure 4-4[B].
33. Connect scope probe to test point TP5 adjust DC BALANCE ADJ R119, CHOPPER BALANCE R155, and TD ADJUST R154 and perform steps 296 through 32 for Channel B. Recheck oscilloscope for dc drift by connecting the scope probe to the phase meter ground and adjusting scope controls to reposition trace on horizontal center line.
34. If steps 25 through 33 have been followed correctly, the digital readout should indicate one half of plus and minus full scale (CALIBRATE switch up and down readings). This reading is called "out of case zero" in the rest of the manual.

Examples:

Calibrate "Up"	Calibrate "Down"	"Out of Case Zero"
+180.0	−180.0	000.0 (±.1°)
+180.2	−179.8	+000.2 (±.1°)
+180.2	−179.4	+000.4 (±.1°)

N O T I C E

Do not be alarmed if the full scale values are not precise, the instrument is out of the case and will return to proper readings when case is replaced. It is important, however, that the "out of case zero" be displaced equally from the range extremes.

DO NOT READJUST FULL SCALE VALUES AT THIS POINT

If "out of case zero" is not equally displaced repeat steps 25 through 33 and step 35 below. Go on to the Zero Crossing High Frequency Procedure; three or four tenths of a degree error could be caused by high frequency misalignment.

N O T I C E

35. Increase the input signal amplitude to both channels to 1 V rms (2.8 V p-p). If reading changes more than ±0.1°, adjust PK-PK ADJ R21 and R112 for accurate time symmetry at test points 2 and 5, as shown in Figure 4-4[C].

4.2.6 Zero-Crossing High-Frequency Procedure

36. Set both VOLTS RMS selectors to .001-2, and RANGE selector to −180°/+180° and remove all scope probes.
37. Apply a 10 mV rms sine wave, 80 kHz, into both channels, using the test configuration shown in Figure 4-1[A].
38. Adjust C22 until digital readout is equally displaced from range extremes for "out of case zero" (±0.2).

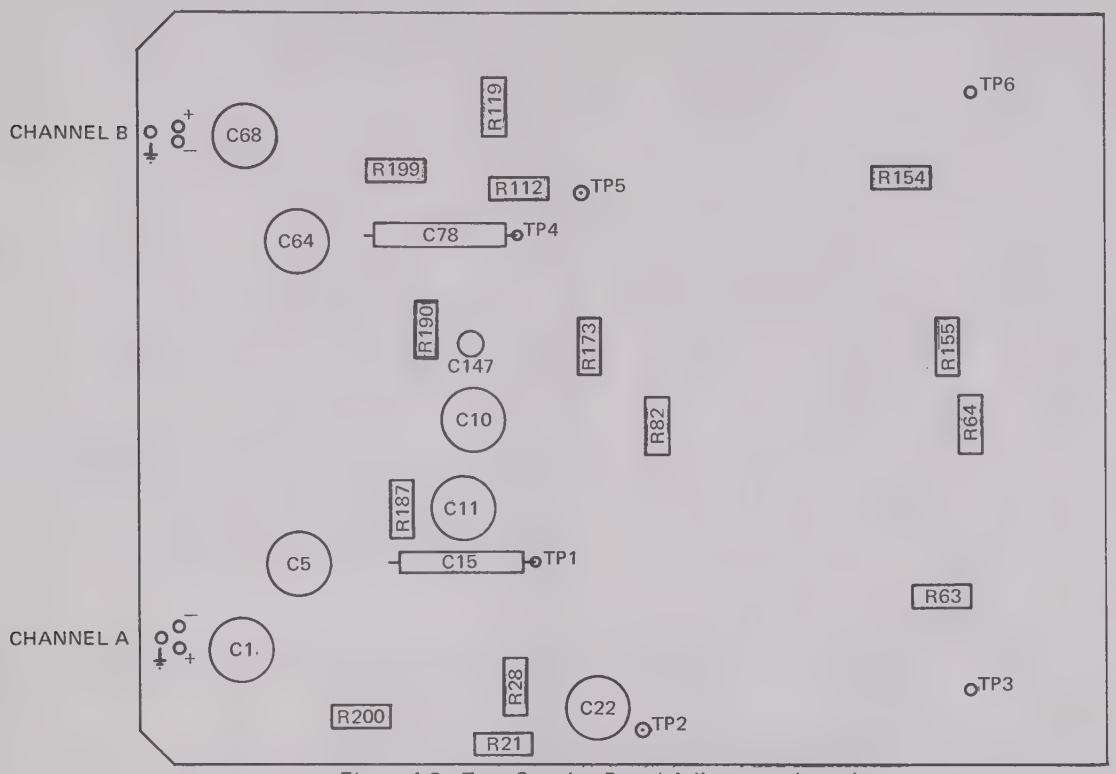


Figure 4-3. Zero Crossing Board Adjustment Locations

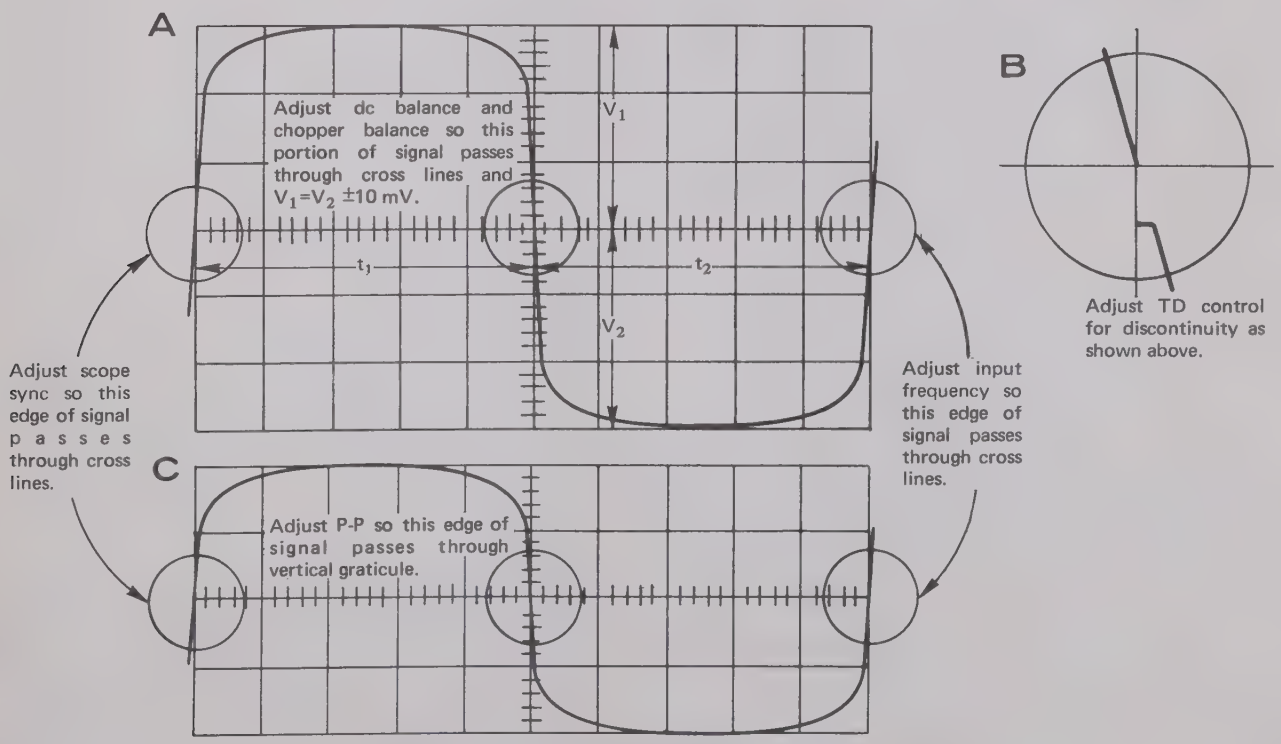

A
Adjust dc balance and chopper balance so this portion of signal passes through cross lines and $V_1=V_2$ ±10 mV.
V_1
V_2
t_1
t_2
Adjust scope sync so this edge of signal passes through cross lines.
Adjust input frequency so this edge of signal passes through cross lines.
B
Adjust TD control for discontinuity as shown above.
C
Adjust P-P so this edge of signal passes through vertical graticule.

Figure 4-4. Oscilloscope Calibration Displays

39. Increase input amplitude to 100 mV rms, increase input frequency to 800 kHz, and adjust C10 until the digital readout equals "out of case zero" (±.4°).
40. Since steps 38 and 39 interact, they must be alternately performed until both readings, when going from one condition to the other, are within limits. Recheck steps 28 through 33 and, if necessary, readjust controls for proper indications.
41. Apply a 1 mV rms sine wave to both inputs, using the configuration shown in Figure 4-1[A] and, while watching the digital readout, vary the frequency from 1 kHz to 10 kHz. Record the reading at 1 kHz and the reading at 10 kHz. Determine the difference between the two readings, taking into account the polarities indicated, and record this as the "error span".

Examples:

1 kHz Readings	10 kHz Readings	Error Span
–000.2	+001.0	1.2°
+000.2	+001.1	.9°
–000.2	–000.8	.6°

42. Set input frequency back to 1 kHz at 1 mV rms and equally adjust Channel A Tunnel Diode ADJ R63 and Channel B Tunnel Diode ADJ R154 so that the digital display readout indicates one-third of the Error Span with a minus sign. (This would be –000.4° in the first example shown in step 41.)
43. Set input frequency to 10 kHz at 1 mV rms and display readout should indicate two-thirds of the Error Span with a plus sign. If the Error Span is not distributed one-third and two-thirds at 1 kHz and 10 kHz respectively, repeat steps 41 and 42.

4.2.6.1 ATTENUATOR FREQUENCY ADJUSTMENT

NOTE

Make sure the oscilloscope probes are properly compensated for lissajous operation. Check each probe with the scope calibrate signal, then connect both probes to the same signal and vary the frequency from 10 Hz to 1 MHz and make final adjustment for closed lissajous.

44. Set both VOLTS RMS selectors to .3-300, and apply a 1 kHz 7 V rms sine wave to the positive input terminals as shown in Figure 4-1[B]. Connect the probes of a dual channel scope, with lissajous capability, between the plus input terminal and test point TP1 of Channel A.
45. While varying the input frequency from 1 kHz to 10 kHz, adjust C1 for a closed lissajous.
46. Connect the scope probes from TP1 to TP4 of Channel B. Adjust C64 for a closed lissajous. The digital readout should now read within ±.2° of reading obtained with 100 Hz input (switch to 100 Hz without changing amplitude and check). If it doesn't, repeat steps 45 and 46 until the readout is within this limit.

4.2.6.2 COMMON MODE REJECTION CALIBRATION

47. Apply a 10 kHz, 10 mV rms, sine wave to both inputs as shown in Figure 4-1[C]; and set VOLTS RMS selectors to .001-2.
48. Connect scope probe to test point TP2, and alternately adjust R187 and C11 for minimum signal. Increase input to 1 V rms and adjust for double input frequency at TP2.
49. Connect scope probe to test point TP5, and alternately adjust R190 and C147 for minimum signal with 10 mV input. Increase amplitude to 1 V rms and adjust for double input frequency at TP5.
50. Repeat steps 47 through 49 using a 100 kHz input. Adjust only variable capacitors for minimum signals at test points.

4.2.6.3 ATTENUATOR COMMON MODE REJECTION ADJUSTMENT

51. Set both VOLTS RMS selectors to .3-300, and apply a 7 V rms 25 Hz sine wave to both inputs as shown in Figure 4-1[C].
52. Connect scope probe to test point TP2, and adjust R200 for minimum signal.
53. Increase input frequency to 25 kHz, and adjust C5 for minimum amplitude at TP2.
54. Connect scope probe to test point TP5, decrease input frequency to 25 Hz, and adjust R199 for minimum signal.
55. Increase input frequency to 25 kHz, and adjust C68 for minimum amplitude at TP5.

NOTE

Above 30 kHz, it is advisable to keep both channels on the same input range (VOLTS RMS) to minimize phase offset differences in the attenuators. If different ranges are used, note offset at 0° and subtract this from the phase reading.

56. Repeat steps 51 through 55 if needed.
57. Replace the dust cover by following the instructions in paragraph 4.1.1; apply POWER, and allow 20 minutes for the unit to reach a stable operating temperature.
58. Check plus and minus full scale calibration on both RANGE selections by applying the same sine wave, 1 kHz at 1 V rms, to both inputs as shown in Figure 4-1[A].

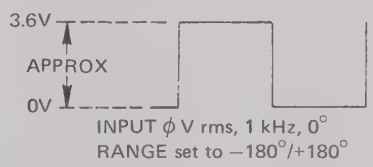
4.3 CORRECTIVE MAINTENANCE

If the Model 750 Phase Meter appears to be operating abnormally, and an investigation of input/output connections, as well as a calibration check, do not cure the problem; follow the trouble-shooting procedure outlined below.

Trouble	Check
1. Readout jumping around when no input signal is applied.	Normal operation, the high sensitivity of the input picks up external 60 Hz noise.
2. Readout scattering occasionally with low input amplitude and/or frequency.	Noise spikes are riding on input signal or signal-to-noise ratio is too high. Put 0.1 μF capacitors, or matched filters, across inputs.
3. Readout scattering randomly with input signal applied.	a. Check that phase angle is not within 2° of RANGE extreme. Use other RANGE setting. b. Reduce ground loops, and use differential inputs isolating grounds.
4. Erroneous phase reading.	a. Check both VOLTS RMS settings. Overdrive causes phase errors. b. Quick check CALIBRATE limits. c. If "a" and "b" do not help, apply same input to both channels, select −180°/+180° RANGE and, if reading is not 000.0, recalibrate Zero Crossing board.
5. Display not lighted when POWER is set to ON.	Check fuse. Check +180 V, ±15 V, ±3.6V, and +5 V power supplies.
6. Two digits light in same lamp.	Defective display lamp.
7. Display locked on maximum or minimum full scale regardless of inputs.	a. If locked on maximum, Channel A Zero Crossing has no output. b. If locked on minimum, Channel B Zero Crossing has no output. c. If not "a" or "b" check IC4 on the Logic and Power Supply board.
8. Input loading circuit being measured due to low input impedance.	Input FET Q1, Q2, Q14, or Q15 has been damaged. Replace with MPF104 or 2N5458 or equivalent.

If the instrument is not operating properly, and the above steps do not solve the problem, recalibrate the instrument as described in paragraph 4.2. If recalibration does not solve the problem, follow the procedure outlined below.

1. First check all power supplies for proper operation. If any are malfunctioning, refer to the Circuit Description as well as the schematic when trouble shooting the supply.
2. With 1 kHz 1 V rms sine waves applied to both inputs, look at Zero Crossing test points TP3 and TP6. If 1 V pulses at 1 kHz are not observed, read Circuit Description and refer to the schematic for trouble shooting.
3. If the proper pulses are seen in step 2 above, look at the junction of R65, R66, and R68. This point should show a waveform like that pictured below.



4. If the dc OUTPUT −10mV/DEG is correct but the digital display is incorrect, recheck +180 V, +5 V, and ±3.6 V supplies. Refer to the timing diagram (Figure 3-6) and Circuit Description given in paragraph 3.2.3.

SECTION 5
NOTES AND ADDENDUMS

5.1 ADDENDUMS

WAVETEK'S product improvement program incorporates the latest electronic development into it's instruments as rapidly as development and testing permit. Due to the time required to document and print instruction manuals, it is not always possible to include the change information in the final printing. When this occurs, change pages or addendum sheets are prepared for insertion immediately behind the title page. If no such pages exist, the manual is correct as printed.

5.2 NOTES

The space below may be used to record pertinent data relating to a specific unit, or general information helpful to user. When minor "special" features are requested in the purchase order, WAVETEK will summarize these features below.

SECTION 6
DRAWINGS AND PARTS LISTS

6.1 SCHEMATIC DIAGRAMS

The schematic diagram(s) within this manual are, whenever possible, positioned opposite the related assembly drawing for maximum information presentation. Additional voltage and/or waveform information, beyond that given in the circuit description, is shown directly on the schematic diagrams, at test points and key locations throughout the instrument.

6.2 ASSEMBLY DRAWINGS AND PARTS LISTS

The following list of manufacturers should be used in conjunction with the parts lists. The abbreviations shown below are used in the "Manufacturer Key" column on the parts lists.

LIST OF MANUFACTURERS

A–B	Allen Bradley
A–E	Arco-Elmenco
AER	Aerovox
ALC	Alco Electronic Products Inc.
AMP	Amp Inc.
APL	Amphenol
APX	Amperex
A–R	American Radionics, Inc.
BEL	Belden
BMC	Budwig Mfg. Co.
BOU	Bourns
B–T	Boots-Townsend Aircraft
BUR	Burroughs
BUS	Bussman
CAM	Cambion
C–D	Cornell Dubilier
CGW	Corning Glass Works
C–J	Cinch Jones
C–K	C and K Components
C–L	Centralab
CTS	Chicago Telephone Systems
C–W	Continental Wire
DEU	Deutsch
DIO	Diodes Inc.
E–C	Electro Cube, Inc.
E–E	Elma Engineering
EFJ	E. F. Johnson Co.
ELC	Elco Corp.
ELP	Elpac Inc.
ETP	Erie Technological Products, Inc.
FCD	Fairchild
G–E	General Electric
G–H	Grayhill
G–R	General Radio Co.
HHS	Herman H. Smith, Inc.
H–P	Hewlett-Packard
IBM	IBM Industrial Products
IMB	IMB Electronics Products
IRC	International Resistance Company
JEF	Jeffers
KEI	Kings Electronics Inc.
LIT	Littelfuse
MAL	Mallory
M–C	Mura Corp.
MEK	Mektron
M–O	Marko-Oak
MOC	Micro-Ohm Corp.
MOL	Molex
MOT	Motorola
M–R	Milton Ross Co.
PPP	Phipps Precision Products
Q–C	Quality Components
QHM	Quality Hardware Mfg.
RCA	Radio Corporation of America
R–E	Richey Electronics
RMC	Radio Material Co.
ROS	Rosan Inc.
R–T	Rubber Teck Inc.
SCC	Stackpole Carbon Co.
SEL	Selectro
SEM	Semtech
S–I	Switchcraft Inc.
SLC	Shur-Lok Corp.
SPR	Sprague
S–T	Sarkes Tarzian
STR	Stettner & Co.
SUP	Superior Electric Co.
SYL	Sylvania
TAS	Teledyne Amelco Semiconductor Co.
T–I	Texas Instruments, Inc.
TRW	TRW Capacitor Division
USE	USECO Inc.
W–E	Wells Electronics
WEI	Wakefield Engineering Inc.

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1		LOGIC & POWER BD	WAVETEK	D750-010	1
2		ANALOG BOARD		D270-011	1
* 3		DIGITAL BOARD		D270 010	1
* 4		ZERO CROSSING BD		D750-011	1
* 5		COVER		D750-311	1
6		FRONT PANEL		C750-300	1
7		FRONT CASTING		B750-302	1
* 8		REAR CASTING		B750-303	1
* 9		REAR PANEL		B750-301	1
10		SIDE PLATES		C130-304	2
* 11		STANDOFFS		A750-313	4
* 12		SHIELD		C740-309	1
13		READOUT BARS		B750-304	2
14		READOUT WINDOW		B750 310	1
15		BRACKET ASSY		D750-001	1
16		BEZEL BAR		B750-305	2
17		FEET	BUDNIG	F68	4
* 18		POWER CORD	BELDEN	17258-S	1
19		SHORTING BAR	G.R.	938-L	2
* 20		HANDLE	QUALITY	1162	1
* 21		CHASSIS BLOCK	WAVETEK	15918-11	2
22					
23		CLIP NUT (#6-32)	SHURE-LOK	SL210-06-2	4
* 24		CAPTIVE SCREWS	DEUTSCH	7900-10-B-2	2
25	J2,3,4 & J7	CONNECTOR (RECEPTACLE / PLUG)	AMPHENOL	DE21BC	6

NOTE: ASTERISK (*) INDICATES ITEM NOT SHOWN

rev	ecn	by	date	app
B	ECN 414	S	8-19-72	S
A	ECN 294	BP	1-23-70	MP

tolerance unless otherwise specified: XXX ± .010, XX ± .030

WAVETEK san diego, calif

scale N/A | by GRAY | date 11-6-69 | app

material: N/A

finish: N/A

title: CHASSIS ASSY

model no. 750 | dwg no. D750-000 | rev B

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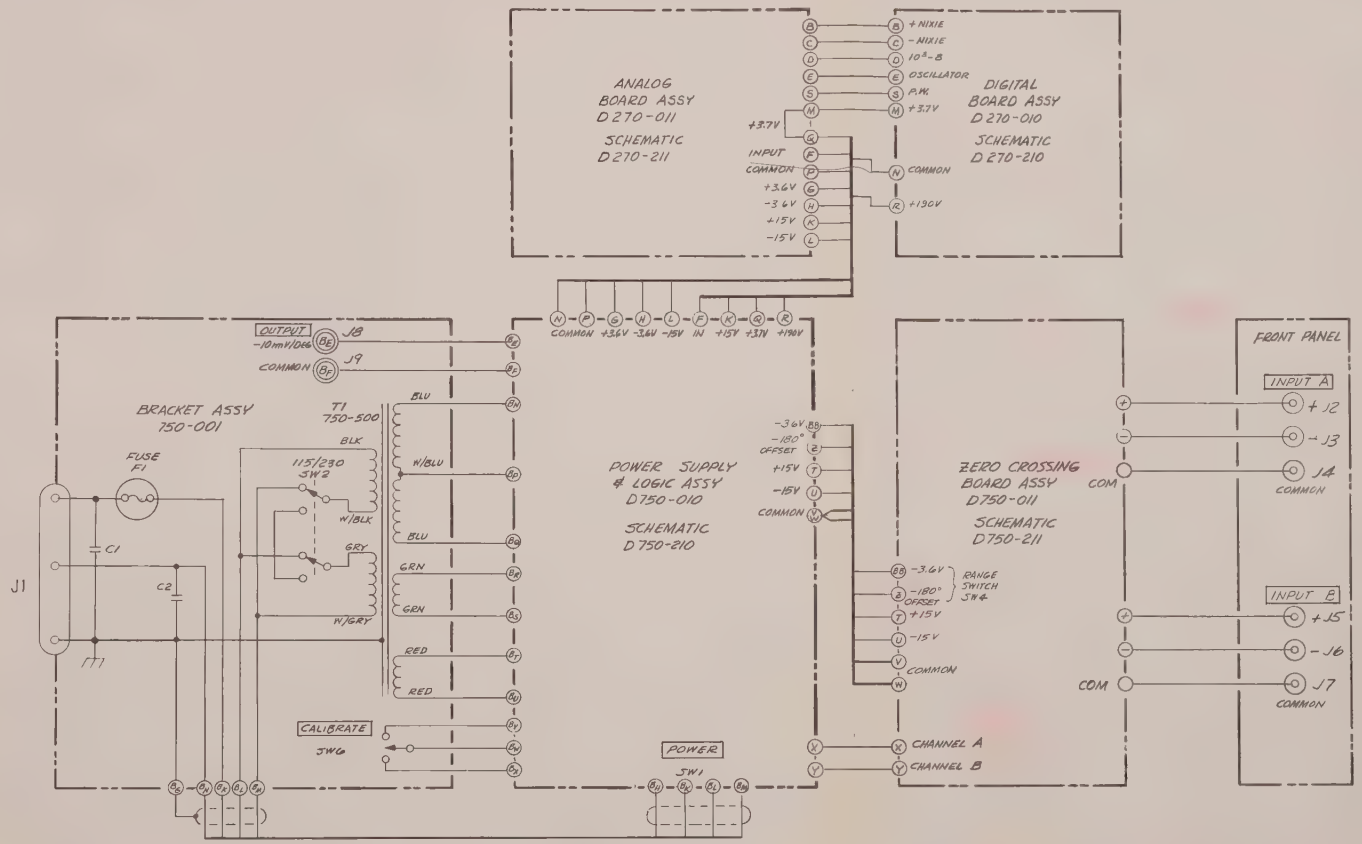

NOTES: UNLESS OTHERWISE SPECIFIED
1. LETTERS ARE INTERCONNECTION POINTS.

tolerance unless otherwise specified .XXX ± .010 .XX ± .030	A	294	NG	1/29/70	
	rev	ecn	by	date	app.
scale NA	WAVETEK san diego, calif.				
material NA	by MAST	date 5 DEC 69	app.		
finish NA	title SCHEMATIC, CHASSIS				
	model no. 750	dwg no. 0750-200	rev A		

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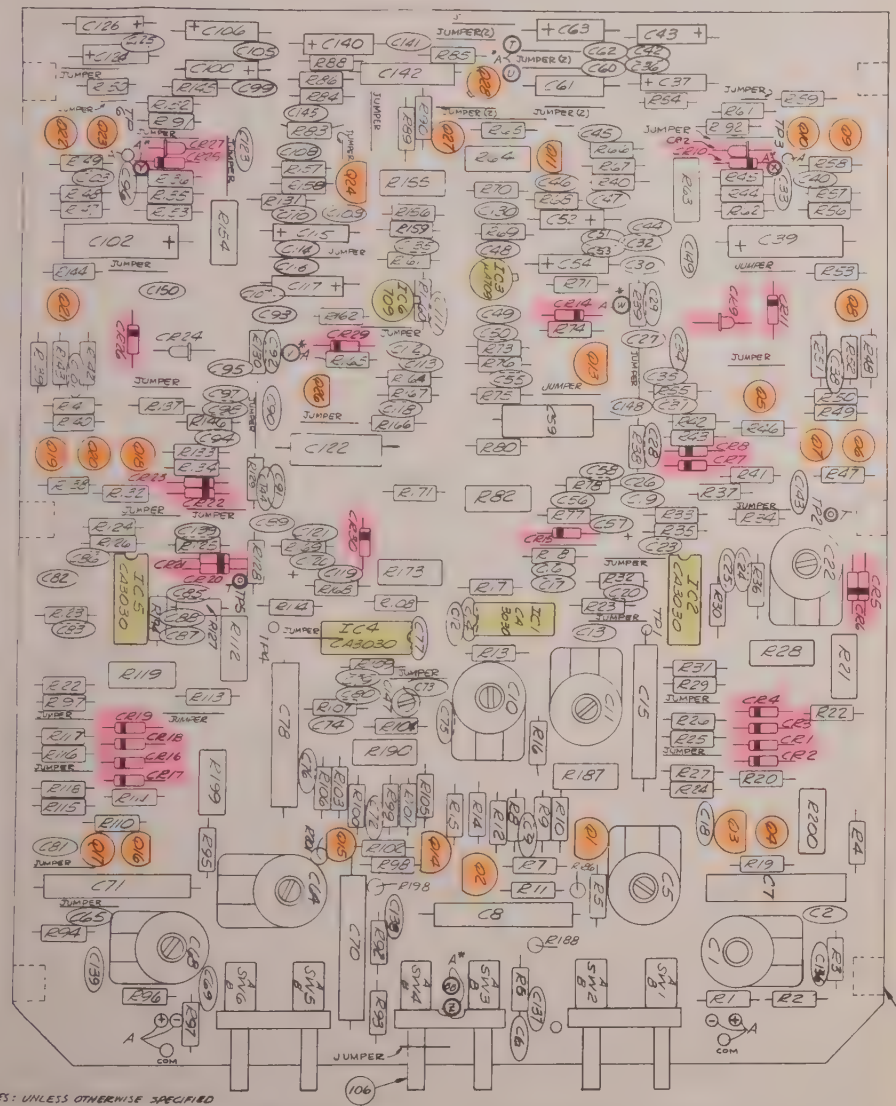

NOTES: UNLESS OTHERWISE SPECIFIED

1. "A" INDICATES AMP PIN MOUNTED ON CIRCUIT SIDE, "A" AMP PIN MOUNTED FROM NEAR SIDE.
2. FOR INTERCONNECTIONS REFER TO SCHEMATIC 750-200
3. LETTER DESIGNATIONS ARE INTERCONNECTION POINTS.

PARTS LIST

NO	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1	C2, C6, C65, C69, C73, C88	CERAMIC DISC 1000V 5 PF	CRL	DD-050	6
2	C130, C135	1.5 PF	SPRAGUE	10TCC-V1S	2
3	C29-C25, C76, C80-C88	10PF	CRL	DD-100	7
4	C18 C81	15PF		DD-150	2
5	C45, C170, C171, C86, C143, C150, C112, C139, C149	22PF		DD 220	7
6	C16, C38, C47, C74, C101, C110	100PF		DD-101	6
7	C48, C111	220PF		DD-221	2
8	C33, C34, C96, C97	330PF		DD-331	4
9	C40, C56, C103, C119	470PF		DD471	4
10	C136-C139	DURA MICA 500V, 1% 910PF(-36)	ARCO	DM15-911F	4
11	C58, C118	CERAMIC DISC 1000V 1500PF	CRL	DD-152	2
12	C28, C30, C91, C93	.08μF		CK-508	4
13	C9, C35, C36, C42, C51, C82, C58, C60, C79, C62, C72, C75, C114, C116, C123, C125, C141, C149, C98, C99	50V .01μF		CK-103	20
14	C12, C13, C19, C20, C31, C44, C45, C50, C52, C73, C76, C80, C83, C84, C101, C108, C113, C121	20V .1μF		UK20-104	18
15	C37, C43, C57, C64, C81, C63, C100, C106, C115, C117, C124, C126, C142	ELECTROLYTIC 15V 5μF	SPRAGUE	500D506G016BA1	13
16	C87, C120	TANTALUM 33μF		196D336X0015FB	2
17	C89, C102	ELECTROLYTIC 16V 100μF		500D107M016DC1	2
18	C59, C122, C142	MYLAR 100V 10% .1μF	CDE	WMF-1P1E	3
19	C7, C8, C15, C70, C71, C78	MYLAR 200V 1% 1μF	ELECTRO CUBE	2101BL-105F	6
20	C155, C101, C27, C64, C68	VARIABLE CAPACITOR 4.5-25PF	ERIE	503-001-37A	7
21	C146	SELECTED VALUE			1
22	C147	VARIABLE CAPACITOR 8.5-15 PF	STETTNER	75-7211K0-02	1
23	C27, C29, C31, C61, C90, C92	CERAMIC DISC 50V .1μF	CRL	CK-104	6
24	C46, C69	MYLAR 50V .1μF	GE	65F92AA/D6	2
25					
26					
27	CR1-CR5, CR7, CR8, CR10, CR14-CR19, CR22, CR23, CR28, CR29, CR30	DIODE	FAIRCHILD	FD6666	18
28	CR11, CR26			1N34A	2
29	CR12, CR27		G.E.	1N3716	2
30	CR9, CR24	TUNNEL		1N3717	2
31	CR5-6, CR20-21	(-42)	H.P.	HP5082-2811	4
32					
33					
34					
35					
36	IC3, IC6	INTEGRATED CIRCUIT	FAIRCHILD	UA709	2
37	IC1 IC4	(-40)	RCA	CA3030	2
38	IC2 IC5	(-40)		CA3030	2
39					
40					
41					
42					
43	Q5 Q10 Q16 Q23	TRANSISTORS	FAIRCHILD	2N3640	4
44	Q4, Q6-Q9, Q11, Q19-Q22, Q27			2N3646	11
45	Q28		MOTOROLA	2N4851	1
46	Q1, Q18, Q24, Q26			MPF-104	4
47	Q1, Q2, Q14, Q15	(-87)		MPF-104	4
48	Q3, Q16	(-38)		MPF-104	2
49					
50					
51					
52	R63, R134	POTENTIOMETER 500Ω	CRL	BA1603-802	2
53	R199, R200	1K		-803	2
54	R21, R192, R190, R187	10K		-805	4
55	R23, R82, R194, R173	100K		-819	4
56	R64, R135	10K	A/B	FR103A1	2
57					

PARTS LIST

NO	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
58	R66 R67	METALFILM 1/4W 1% 46.4Ω	CORNING	RN60D	2
59	R62, R68, R139, R136	8.82K			4
60	R42, R43, R138, R184	4.99K			4
61	R6 R98	9.53K			2
62	R2 R95	10K			2
63	R14, R15, R105, R106	10K(-4)			4
64	R96	12.1K			1
65	R13, R16, R104, R107	12.1K(-33)			4
66	R40 R181	27.4K			2
67	R7 R11, R44, R102	1MΩ			4
68	R1, R5, R42, R96	1MΩ(-34)			4
69					
70					
71					
72	R48, R54, R71, R73, R88, R180, R145, R162, R164	CARBON 1/2W 5% 47Ω	STACKPOLE	RC20GF470J	9
73	R84	68Ω		680J	1
74	R3, R9, R19, R32, R88, R94, R97, R110, R123, R149,	10% 100Ω		101K	10
75	R41 R182 R197 R139	150Ω		151K	4
76	R47, R85, R87, R130, R146, R148	470Ω		471K	6
77	R44 R101 R67, R76 R83, R136 R138, R150 R154,	1K		102K	11
78	R17, R18, R33, R38, R89, R91, R98, R105, R179, R126, R129, R152, R160	1.5K		152K	13
79	R53, R90, R144	2.2K		222K	7
80	R8 R99	2.7K		272K	2
81	R191 R192	3.3K		332K	2
82	R34 R125	3.9K		392K	2
83	R22, R30, R66, R69, R92, R113, R135, R140, R143, R144	4.7K		472K	10
84	R25 R116	5.6K		562K	2
85	R10, R12, R101, R103	6.8K		682K	4
86	R9 R100	7.5K		752K	2
87	R24	9.1K		912K	1
88	R20, R26, R27, R51, R86, R77, R86, R111, R117, R118, R142, R147, R168, R171	10K		103K	14
89	R24 R115	22K		223K	2
90	R46 R137	27K		273K	2
91	R31, R33, R75, R122, R124, R166	47K		473K	6
92	R30 R141	62K		623K	2
93	R76 R167	150K		154K	2
94	R74 R165	220K		224K	2
95	R23 R116	470K		474K	2
96	R37-R39, R128-R130	1MΩ		05K	6
97	R70 R161	2.2MΩ		225K	2
98					
99					
100		CIRCUIT BOARD	WAVETEK	740-111E	1
101					
102	⊙	TERMINALS	USECO	20108-1	8
103					
104	○A	AMP PINS	AMP	61182-2	16
105					
106	SW1-SW6	SWITCH ASSY	WAVETEK	B750-400	3
107		CHASSIS FASTENER	USECO	15918-1	6

B	ECN 413	S	7/11/72	S	
A	ECN 294	BS	1-22-70		

tolerance unless otherwise specified .XXX ± .010 .XX ± .020

scale N/A

material N/A

finish N/A

rev	ecn	by	date	app

WAVETEK san diego, calif

by ROCHICHIO date 11-22-69 appr

title ASSY ZERO CROSSING BD

mode. no 750 | dwg no D750-011 | rev B

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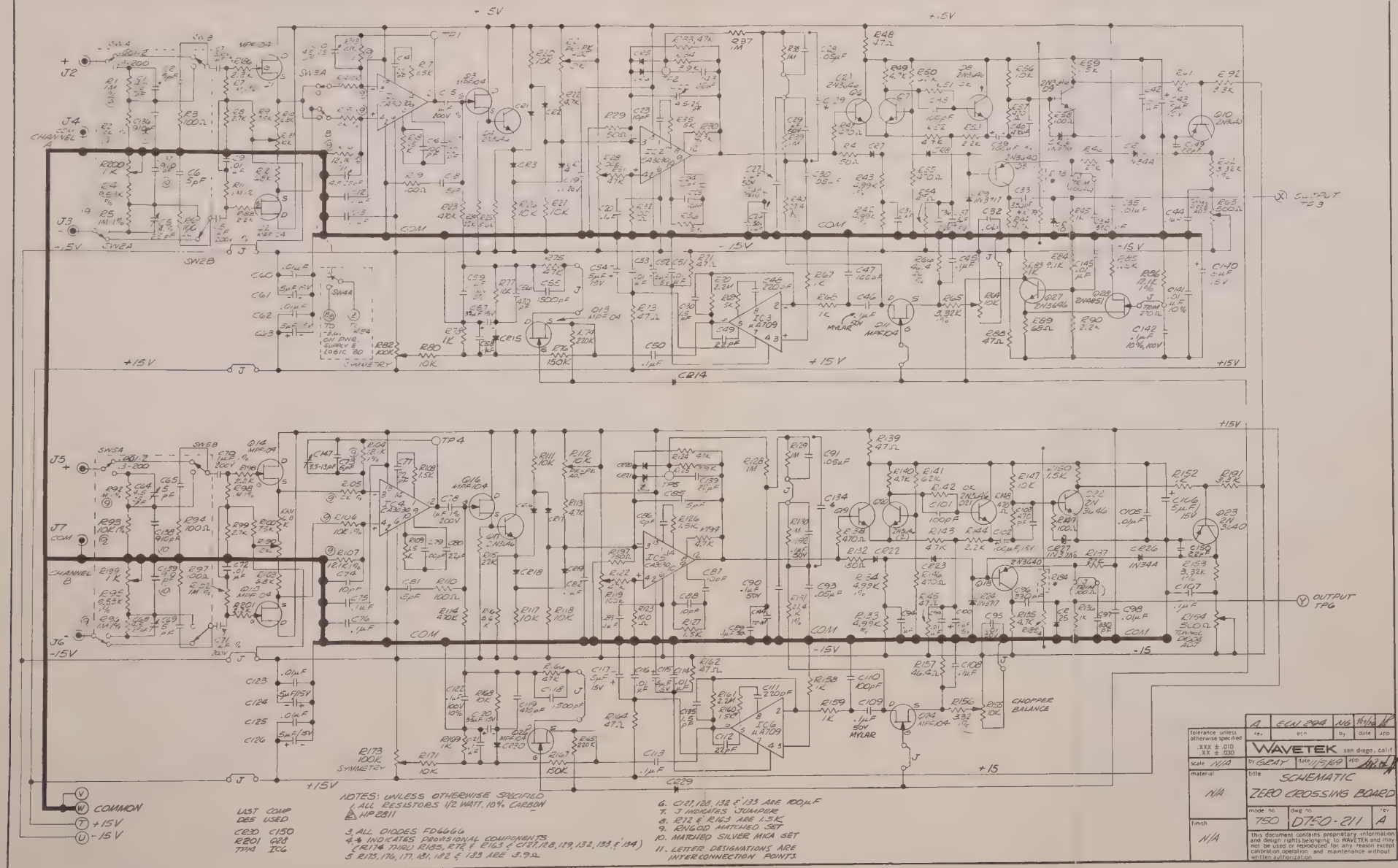
+5V
+15V
-15V
J2
J4
CHANNEL A
J3
SW1A
SW1B
SW2A
SW2B
TP1
TP2
TP3
OUTPUT
COM
CHANNEL B
J5
J6
J7
TP4
SYMMETRY
CHOPPER BALANCE
MYLAR
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS 1/2 WATT, 10% CARBON
2. HP2811
3. ALL DIODES FD6666
4. % INDICATES PROVISIONAL COMPONENTS
5. R135, 176, 177, 181, 182 & 183 ARE 3.9Ω
6. C127, 128, 132 & 133 ARE 100μF
7. J INDICATES JUMPER
8. R72 & R163 ARE 1.5K
9. XENGOD MATCHED SET
10. MARKED SILVER MICA SET
11. LETTER DESIGNATIONS ARE INTERCONNECTION POINTS
LAST COMP DES USED
C230 C150
R201 Q28
TP14 IC6
COMMON
+15V
-15V
A ECN 294 NG 11/4/69
WAVETEK san diego, calif
SCHEMATIC
ZERO CROSSING BOARD
model no. 750
dwg no. D750-211
rev. A
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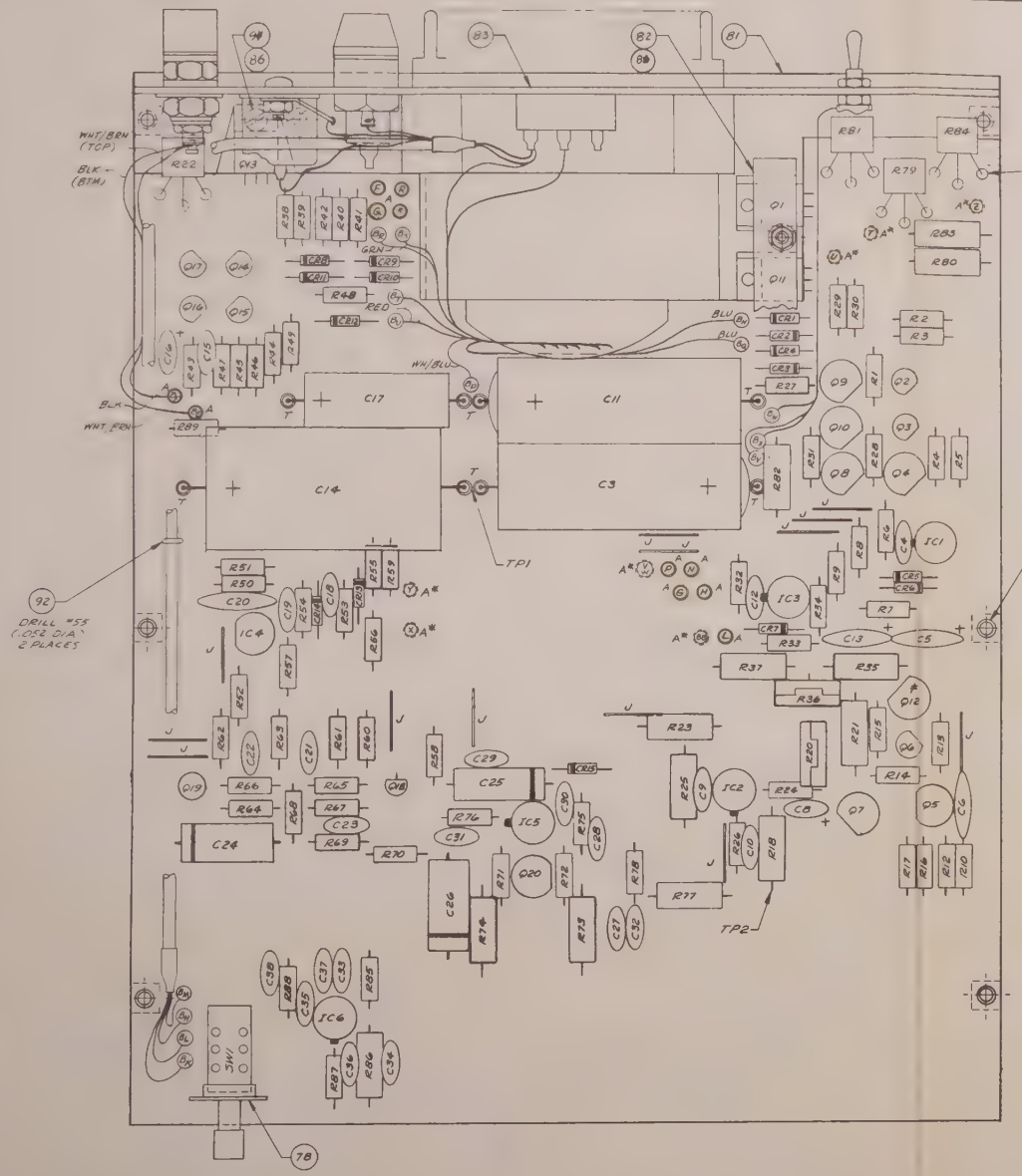

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1	C13,C19,C21 C22.	CERAMIC DISC .1KV 22PF	CRL	DD220	4
2	C9,C30,C35	220PF		DD221	3
3	C4,C10,C14 C15,C28,C31 C32,C34 C36,C38	50V .005μF		CK502	10
4	C27,C29 C33,C37	.01μF		CK103	4
5	C6,C20 C23	20V .1μF		UK-20-104	3
6	C24,C25,C26	MYLAR 200V .33μF	TRW	K463F	3
7	C5,C13	TANTALUM 35V 27μF	SPRAGUE	196D276X0035FB	2
8	C8,C16	15V 33μF		196D336X0015FB	2
9	C17	ELECTROLYTIC, 350V 4μF	CDE	BR-4-350	1
10	C3,C11	35V 10000μF	SPRAGUE	TVA10005355LC4	2
11	C14 /5	15V 4000μF	RICHEY	34-1000-4000-R7	1
12					
13					
14					
15	CR5,CR6 CR7,CR15	DIODE FD6666	FAIRCHILD	FD6666	4
16	CR13,CR14	HP2811	HP	HP5082-2811	2
17	CR1,CR2,CR3 CR4,CR8,CR9 CR10,CR11	SCE-1	SEMTECH	SCE-1	8
18	CR12	SCE-2	SEMTECH	SCE-2	1
19	IC1,IC2,IC3 IC5,IC6	INTEGRATED CIRCUIT	FAIRCHILD	μA709	5
20	IC4		CyL914		1
21					
22	R20	POTENTIOMETER 100Ω	CRL	BA1603-801	1
23	R36	1K		BA1603-803	1
24	R22,R29,R81	TYPE S 50Ω (-41)	AB	SV5011	3
25	R84	1K (-45)		SV1021	1
26					
27					
28	R40,R61	CARBON, 1/2W, 10% 9.9Ω	STACKPOLE	RC20GF389K	2
29	R2,R30,R58	6.8Ω		6R8K	3
30	R52	33Ω		330K	1
31	R46 R78, R88	100Ω		101K	3
32	R17, R42 R50, R51	330Ω		331K	4
33	R3,R28	470Ω		471K	2
34	R43	680Ω		681K	1
35	R45, R61 R62, R89	1K		102K	4
36	R6,R8,R32 R35,R59 R74, R87	1.5K		152K	7
37	R12,R53,R54	1.8K		182K	3
38	R47	2.2K		222K	1
39	R1,R4,R5,R9 R21,R28,R31 R33,R39,R44 R45,R46,R47	4.7K		472K	13
40	R13	5.6K		562K	1
41	R60,R63	15K		153K	2
42	R56,R57	47K		473K	2
43	R49	1M		105K	1
44	R88	CARBON 1/2W, 10% 1.2K		122K	1
45					

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
46	R71,R72	METAL FILM 1/4W 1% 1K	CENTRALAB	RN60D	2
47	R14	2.37K			1
48	R44	4.99K			1
49	R34,R85	3.32K			2
50	E24	4.75K			1
51	R10,R14	5.76K			2
52	R7,R8,R38	10K			3
53	R15	19.1K			1
54	R48,R69,R70	237K			3
55	R75	698K			1
56	R73,R74	1/2W 1% 2M		RN65D	2
57					
58					
59	R18	WIRE WOUND PRE AGED 1/4W 237K (-35)	MILROY OHM	TYPE 149	1
60	R35	900K (-35)			1
61	R77	9.53K (-35)			1
62	R23	9,75K (-35)			1
63	R21,R25,R37 R80,R86	10K (-35)			5
64	R82,R83	19.6K (-35)			2
65					
66					
67	Q1, Q13	TRANSISTOR TIP29	TI	TIP29	2
68	Q11	TIP30		TIP30	1
69	Q2,Q3,Q6,Q14, Q15,Q16,Q17	2N3565	FAIRCHILD	2N3565	7
70	Q4,Q8,Q9 Q10	2N3638		2N3638	4
71	Q18	2N3640		2N3640	1
72	Q7	2N3642		2N3642	1
73	Q19 /5	2N3646		2N3646	1
74	Q5, Q20	TD101	SPRAGUE	TD101	2
75	Q12	(-39)	FAIRCHILD	2N3638	1
76					
77					
78	SW1	SWITCH ASSY, PUSH-PUSH	HAVETER	740-400	1
79					
80					
81		CIRCUIT BOARD	WAVETEK	740-110	1
82		HEATSINK		130-311	1
83		BRACKET ASSEMBLY		750-001	1
84					
85					
86		TRANSISTOR INSULATOR	WAVETEK	740-307	1
87		AMP PIN	AMP	61182-2	18
88		CHASSIS FASTENER	USECO	15918-1	6
89		TERMINAL		20108-1	8
90		TERMINAL		20058-1	12
91		TRANSIPADS	MILTON BOTT	10123N	6
92		MOUSE TAIL	RUBBER TECK	2829-33-2	1
93		SCREW, NYLON 6-32	WH SMITH	2505	1
94		INSULATOR	WAVETEK	142-311	1

NOTES: UNLESS OTHERWISE SPECIFIED.

1. FOR INTERCONNECTIONS REFER TO SCHEMATIC 750-200.
2. J INDICATES JUMPER.
3. T INDICATES TERMINAL.
4. A INDICATES AMP PIN MOUNTED FROM NEARSIDE; A* INDICATES AMP PIN MOUNTED ON CIRCUIT SIDE.
5. NO SUBSTITUTION SHALL BE ALLOWED FOR PART INDICATED.
6.
7. LETTER DESIGNATIONS ARE INTERCONNECTION POINTS.

rev	ecn	by	date	app
E	ECN 473	S	3/4/71	S
D	ECN 390	[illegible]	4/6/71	[illegible]
C	ECN 375	BOB	11-2-70	[illegible]
B	ECN 306	WB	9/30/70	[illegible]
A	ECN 294	BO	1/29/70	[illegible]

tolerance unless otherwise specified .XXX ± .010 XX ± .030

scale 2X

material NA

finish NA

WAVETEK san diego, calif

by MAST date 6 NOV app [illegible]

title ASSEMBLY, POWER SUPPLY & LOGIC

model no. 750 dwg no. D750-010 rev E

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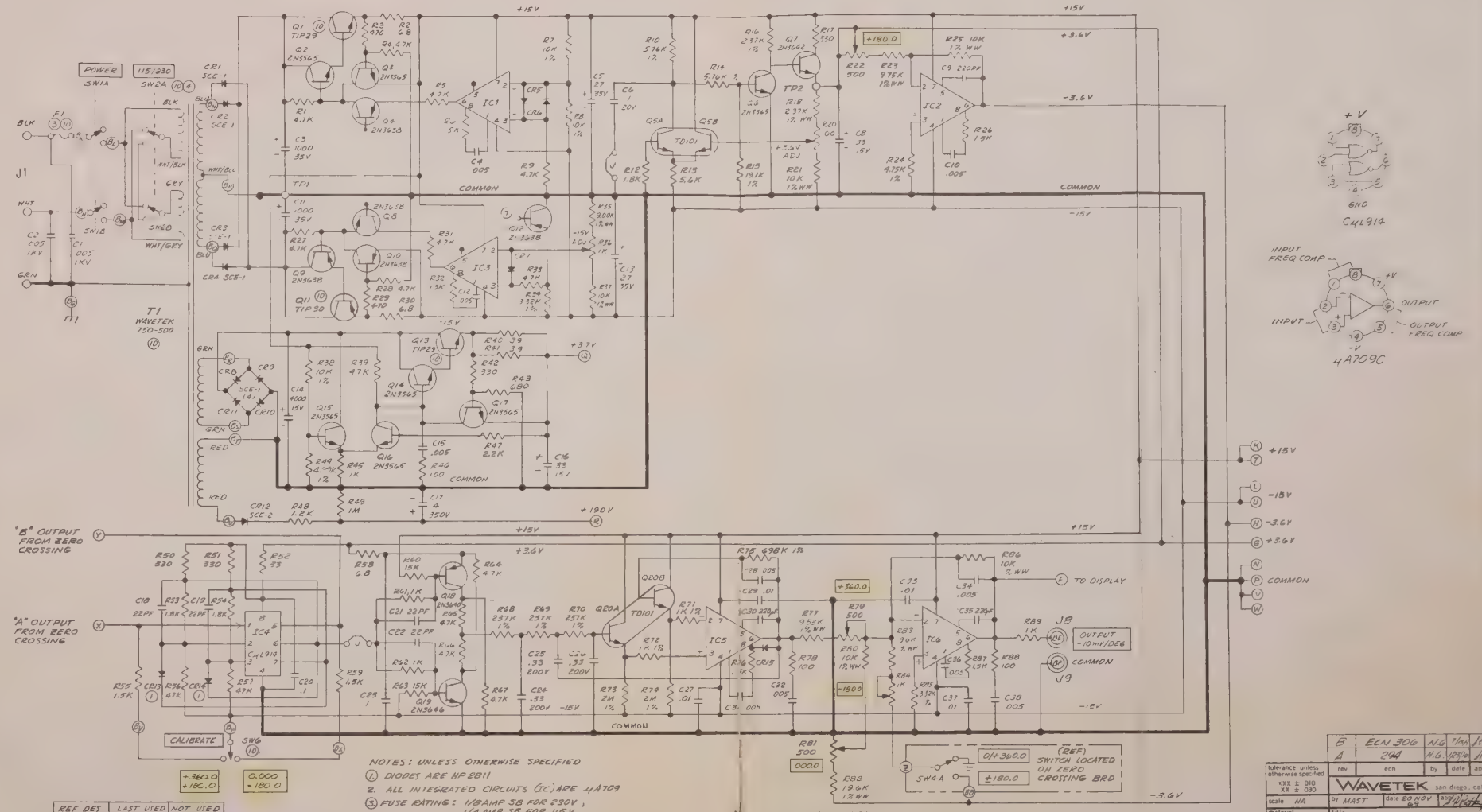

REF DES	LAST USED	NOT USED
DIODE	CR15	—
CAPACITOR	C38	C7
INTEGRATED CIRCUITS	IC6	—
TRANSISTOR	Q20	—
RESISTOR	R89	R11, R19
SWITCH	SW6	SW3, SW5

NOTES: UNLESS OTHERWISE SPECIFIED

1. DIODES ARE HP 2811
2. ALL INTEGRATED CIRCUITS (IC) ARE 4A709
3. FUSE RATING: 1/8 AMP SB FOR 230V, 1/4 AMP SB FOR 115V.
4. SWITCH SHOWN IN 115V POSITION.
5. J INDICATES JUMPER.
6. ALL DIODES ARE FDG666.
7. SELECTED
8. ALL RESISTORS ARE CARBON, 1/2 WATT, 10%; VALUE IN OHMS.
9. CAPACITOR VALUES ARE IN MICROFARADS.
10. COMPONENTS ARE MOUNTED ON REAR BRACKET ASSEMBLY.
11. LETTER DESIGNATIONS ARE INTERCONNECTION POINTS.

B	ECN 3006	N.G.	7/1/71	JP
A	2991	N.G.	10/4/70	JP
rev	ecn	by	date	app.

tolerance unless otherwise specified: XXX ± .010, XX ± .030

WAVETEK san diego, calif

scale NA | by MAST | date 20 NOV 69 | app

material: NA

title: SCHEMATIC, POWER SUPPLY & LOGIC

model no 750 | dwg no D750-210 | B

fin sh: NA

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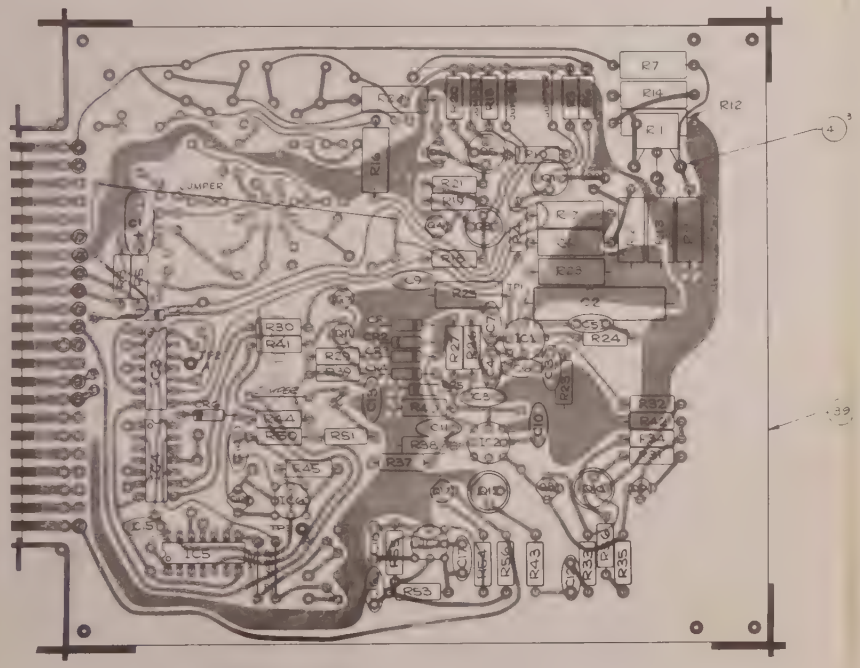
JUMPER
R7
R14
R12
R1
R16
R23
R28
R24
R30
R41
R29
R40
R32
R42
R31
R43
R45
R51
R37
R53
R54
R56
R33
R35
IC1
IC2
IC3
IC4
IC5
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
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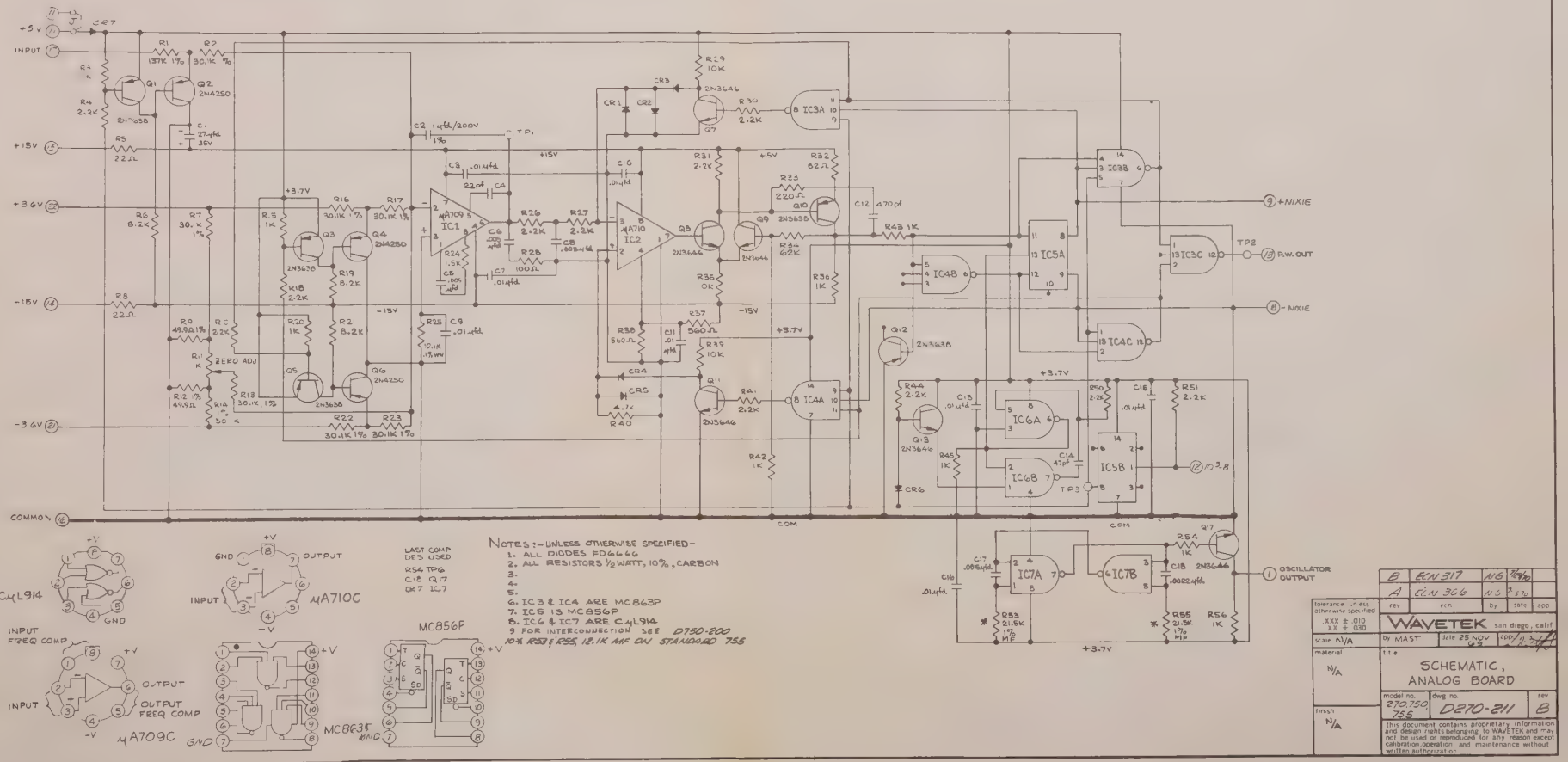
C36
C37
C38
C39
C40



C4L914

µA710C

µA709C

MC8638

MC856P

LAST COMP DES USED
R54 TP6
C18 Q17
CR7 IC7

NOTES :- UNLESS OTHERWISE SPECIFIED-
1. ALL DIODES FDG666
2. ALL RESISTORS ½ WATT, 10%, CARBON
3.
4.
5.
6. IC3 & IC4 ARE MC863P
7. IC5 IS MC856P
8. IC6 & IC7 ARE C4L914
9 FOR INTERCONNECTION SEE D750-200
10% R53 & R55, 12.1K MF ON STANDARD 755

B	ECN 317	NG	3/29/70	
A	ECN 306	NG	2/5/70	
rev	ecn	by	date	app

tolerance unless otherwise specified: XXX ± .010, XX ± .030

WAVETEK san diego, calif

scale N/A | by MAST | date 25 NOV 69 | app'd

material: N/A

finish: N/A

title: SCHEMATIC, ANALOG BOARD

model no. 270,750 755 | dwg no. D270-211 | rev B

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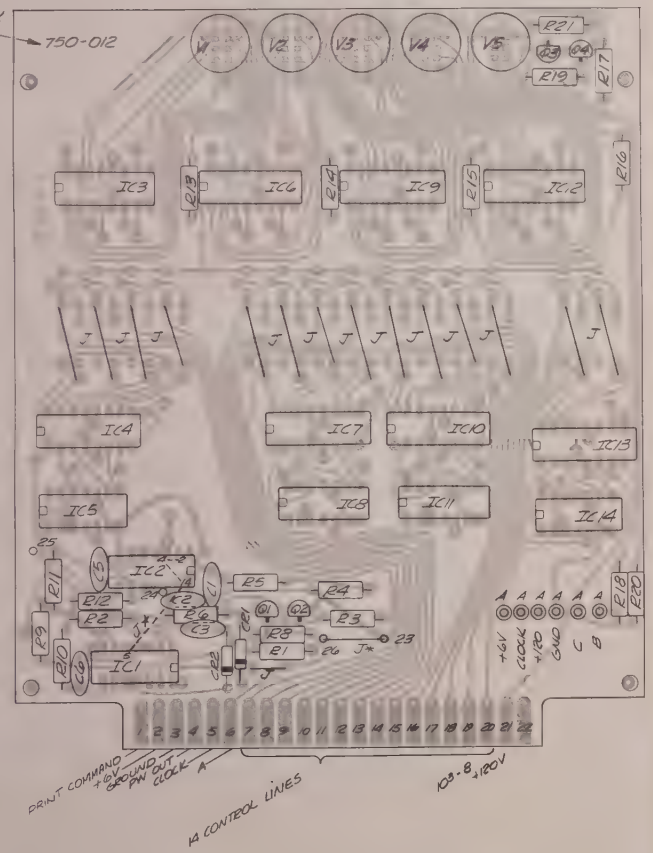

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPS MUST HAVE STRAIGHT LEADS
2. J* INDICATES MOUNTED ON CIRCUIT SIDE
3. J* INDICATES MODEL 750 ONLY

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO.	QTY
1		CAPACITORS			
2	C1, C2, C3, C6	CERAMIC DISC, 1 KV, 10%, .004μF	CRL	DD102	4
3					
4	C5	10V 0.47μF	SPRAGUE	NY-325	1
5					
6					
7					
8					
9		DIODES			
10	CR1, CR2	FD6666	FAIRCHILD	FD6666	2
11					
12					
13					
14		INTEGRATED CIRCUITS			
15	IC1, IC2	QUAD 2 INPUT NAND	MOTOROLA	SN7400	2
16	IC3, IC6, IC9, IC12	DECODER DRIVER		7441	4
17	IC4, IC7, IC10, IC13	QUAD LATCH		7475	4
18	IC5, IC8, IC11, IC14	DECADE COUNTER		7490	4
19					
20					
21					
22	V1-V4	NIXIE TUBES 0-9	BURROUGHS	B5750	4
23	V5	+, -		B5856	1
24					
25		RESISTORS			
26	R1, R3, R11, R12	CARBON, 1/2W, 10% 2.2K	STACKPOLE	RC20GF222K	4
27	R5	4.7K		472K	1
28	R18, R20	10K		103K	2
29	R13-R17	18K		183K	5
30	R9, R10	47K		473K	2
31	R2, R4, R6, R8	5% 750Ω		75.J	4
32	R19, R21	10% 1M		105K	2
33					
34					
35					
36					
37	Q1, Q2	TRANSISTORS 2N3646	MOTOROLA	2N3646	2
38	Q3, Q4	MPS L01		MPS L01	2
39					
40					
41					
42					
43	ⓐ A	AMP PINS	AMP	61182-2	6
44					
45					
46					
47					
48		DIGITAL BOARD	WAVETEK	750-112A	1
49					
50					

rev	ecn	by	date	app
D	ECN 313	NG	1/8/71	
C	ECN 325	NG	12/8/70	
B	ECN 316	NG	12/1/70	

tolerance unless otherwise specified XXX ± .010 XX ± .030

scale N/A

material N/A

finish N/A

WAVETEK san diego, calif

by BRUCHNO date 4-20-70 app.

title ASSY DIGITAL BOARD

model no. 750/755 dwg no. 0750-012 rev D

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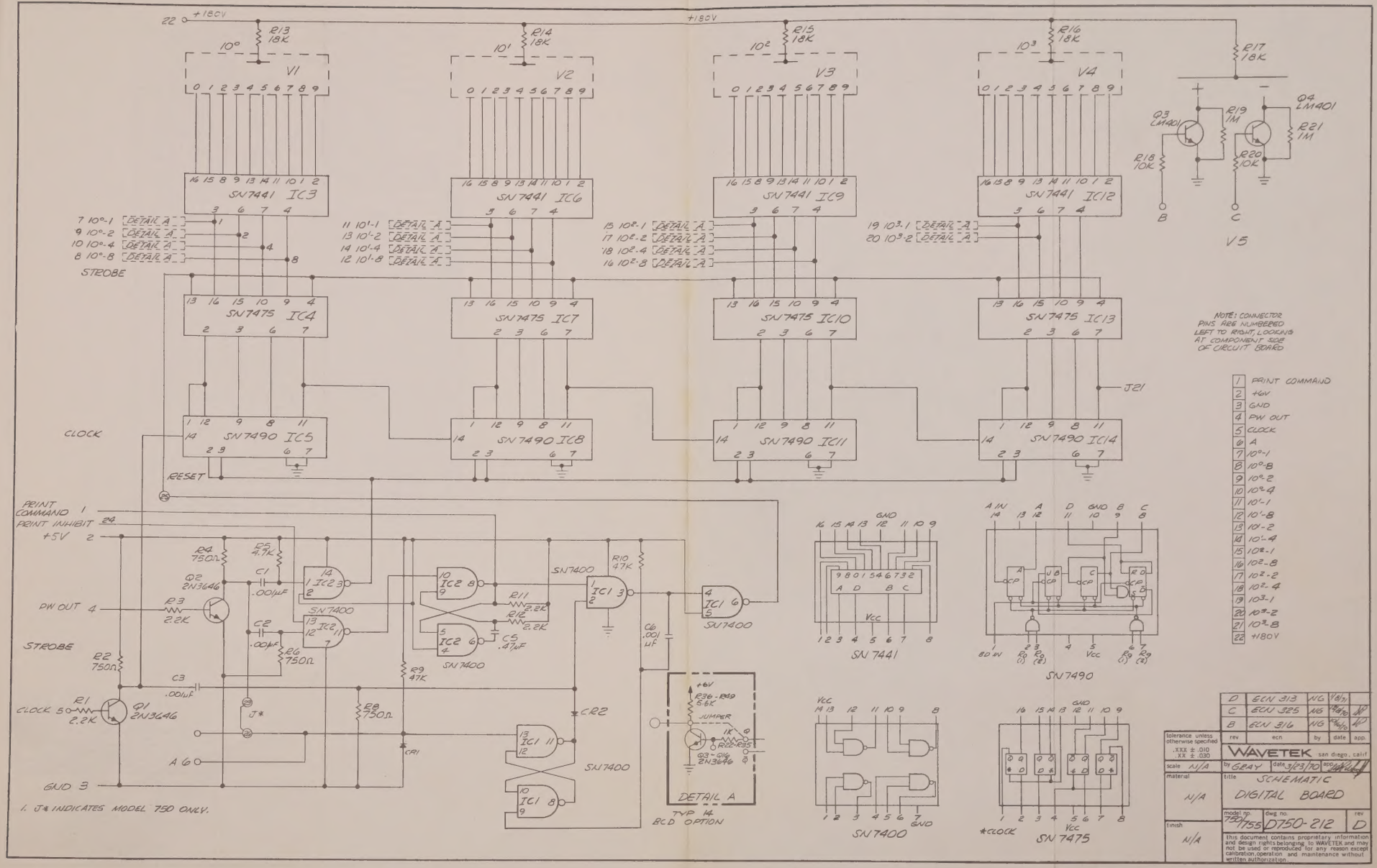

D	ECN 313	NG	10/1/	
C	ECN 325	NG	9/16/70	JW
B	ECN 316	NG	4/6/70	AP
rev	ecn	by	date	app.

tolerance unless otherwise specified .XXX ± .010 .XX ± .030
scale N/A
material N/A
finish N/A

WAVETEK san diego, calif
by GRAY date 3/23/70 app.
title SCHEMATIC DIGITAL BOARD
model no. 750/755 dwg no. D750-212 rev D

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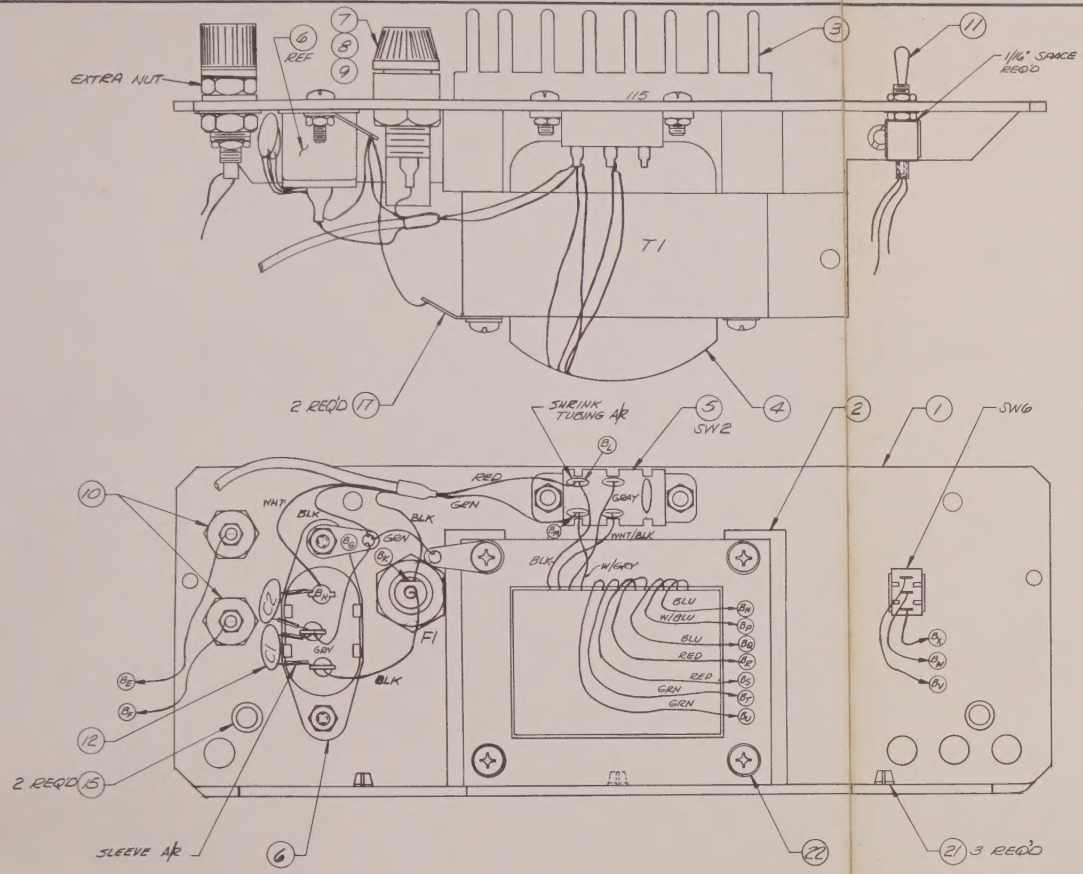

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO.	QTY
1		BRACKET	WAVETEK	C750-304	1
2		TRANSFORMER MTG BAR		A750-307	2
3		HEATSINK		B750-309	1
4	T1	TRANSFORMER	WAVETEK	C750-500	1
5	SW2	LINE SWITCH 115/230	SWITCH-CRAFT	46256LF SOLDER LUGS	1
6	J1	POWER CORD RCPT		LAC36	1
7	F1	FUSE HOLDER	LITTELFUSE	342012	1
8		FUSE 1/4 AMP ASB		313-250	1
9		FUSE 1/8 AMP 230V		313-125	1
10	J8, J9	BINDING POST	E.F. JOHNSON	111-103	2
11	SW6	SWITCH SPDT MOMENTARY	C-K	T63-7105	1
12	C1, C2	CAPACITOR, 1KV, .005μF	CRL	DD502	2
13					
14					
15		PRESS NUT	BOSAN	MRFN-10-32	2
16					
17		SOLDER LUG	H.H. SMITH	1414-6	2
18					
19					
20					
21		#6-32 FASTENER	BOOTS AIRCRAFT	TB1000TO-632	3
22					

NOTES: UNLESS OTHERWISE SPECIFIED
1. FOR INTERCONNECTIONS REFER SCHEMATIC 750-200
2. LETTER DESIGNATIONS ARE INTERCONNECTION POINTS.
3. WIRE COLORS INDICATED ARE FOR REFERENCE ONLY.

rev	ecn	by	date	app.
C	ECN 413	S	7/11/72	S
B	COP 29	NS	5/20/70	
A	ECN 294	BL	1/20/70	

tolerance unless otherwise specified .XXX ± .010 .XX ± .030

WAVETEK san diego, calif

scale N/A

by GRAY date 10/24/69

material N/A

finish N/A

title ASS'Y, BRACKET

model no. 750

dwg no. 0750-001

rev C

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